A 170 nW CMOS Wake-Up Receiver with -60 dBm Sensitivity Using AlN High-Q Piezoelectric Resonators

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***Abstract*—A new wake-up receiver (WuRx) designed in 0.13 µm CMOS process is hybrid-integrated with a microelectromechanical system (MEMS) RF resonator. While only consuming 166 nW of power (18.8 nW for the comparator and 147 nW for periphery), the WuRx is capable of detecting RF signals as weak as -60 dBm. In order to achieve this sensitivity, a passive voltage-boosting network comprised of a high quality factor (high-Q) piezoelectric MEMS resonator is utilized, in place of an inductor, to amplify the received voltages applied to a CMOS rectifier. The output of the rectifier is then applied to a low-power comparator used to set a logical bit that indicates when an RF signal has been detected. The trade-offs in designing the voltage boosting network are explained and an equation for the optimum number of rectifier stages is derived.**

I. Introduction

Wake-up receivers are an essential part of wireless sensor networks, used in applications such as Internet of Things, Ambient Intelligence, and Personal Area Networks [1–4]. One of the most important challenges in designing a wake-up receiver (WuRx) is to minimize power consumption to extend battery life. Aggressive duty-cycling is commonly used to lower the power consumption, but requires an always-on low-power front-end to enable this cycling. A CMOS rectifier can be used in a radio frequency (RF) WuRx to convert the received attenuated RF signal to a DC voltage in steady state. The change in voltage can then be detected by a comparator to indicate when an RF signal has been received. Typically, the interface between the antenna and the CMOS rectifier is a power matching network (PMN) that maximizes power transfer, but not necessarily the voltage seen at the rectifier input, which limits the minimum detectable signal.

Alternatively, a passive voltage boosting network can be incorporated as the interface between the antenna and the CMOS rectifier [5], which can improve the sensitivity but is strongly dependent upon the quality factor (Q) of the passive components. Q is typically low in CMOS processes which leads to the use of an off-chip high-Q inductor to improve performance at the cost of increasing the size of the WuRx. In this work, a high-Q MEMS piezoelectric resonator replaces the inductor used in the voltage-boosting circuit resulting in a larger voltage seen by the CMOS rectifier. The increase in voltage to the rectifier results in a larger steady-state DC voltage being sensed by a fully differential comparator in negative feedback. The high-Q piezoelectric resonators can be fabricated in an AlN MEMS process, AlN plate sandwiched between Mo (bottom) and Al (top), that is eutecticly bonded to a 0.18 µm CMOS die [6]. This monolithic structure can then be wire bonded to the 0.13 µm WuRx implemented in this work.

II. Voltage-Boosting

Diode-connected MOSFETs are used in the construction of a rectifier (Fig. 1a). The input impedance of the n-stage rectifier is capacitive and defined by $Z_{in} = R_n - jX_n$, given $R_n = R_1 \div n$ and $X_n = X_1 \times n$; where R_1 and X_1 are the resistance and reactance of each stage. A large mismatch between the impedances of the rectifier and antenna (R_{ant}) affects performance drastically. Conventionally, a PMN is utilized between the antenna and the rectifier stage to maximize power transfer, but when implemented in CMOS processes the components have finite-Q limiting the minimum detectable RF power. PMN can be modeled by a parallel RC circuit, $R_p = {}^{(R_n^2+X_n^2)}/_{R_n} \gg 50\,\Omega$.

Instead, a single inductor can be used between the antenna and rectifier to boost the voltage via resonating with the input capacitance of the rectifier. The voltage phasor at the rectifier input can be written as:

$$V_{in} = \frac{\sqrt{R_n^2 + X_n^2}}{R_n + R_{ant}} V_{RF} \approx \frac{X_n}{R_n + R_{ant}} V_{RF} \quad (1)$$

Equation (1) implies, the greater the ratio of the reactance of the rectifier to $(R_n + R_{ant})$ the higher voltage

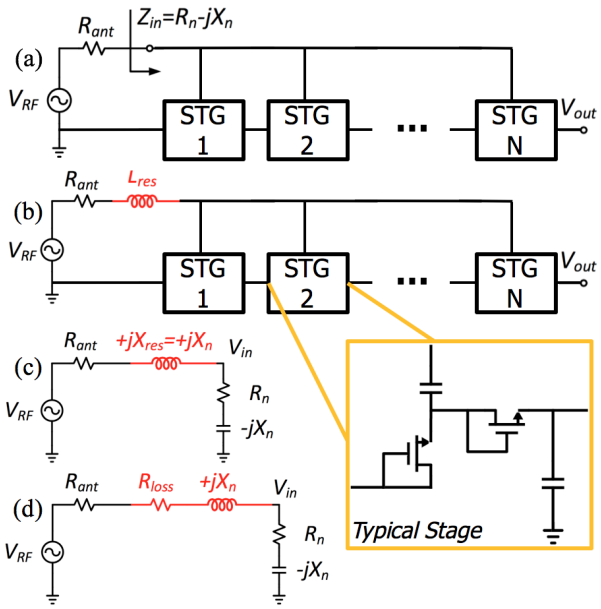

Fig. 1: (a) N-stage MOS rectifier connected to an antenna, (b) incorporation of a series inductor as a voltage boosting network to increase signal, (c) series *RLC* circuit model, and (d) lossy series inductor model.

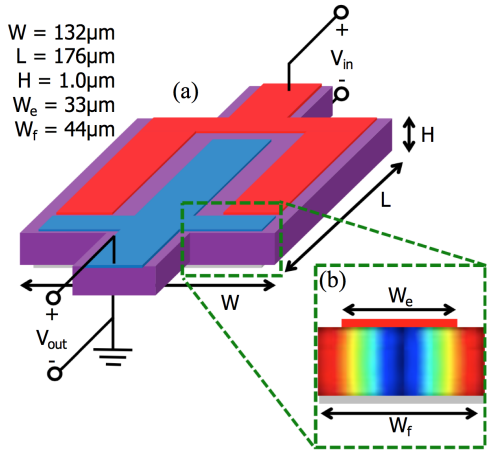

Fig. 2: (a) 2-port piezoelectric laterally-vibrating MEMS resonator and (b) cross-section of one finger exhibiting a width-extensional mode of vibration [6–8].

boosting. This approach can improve the sensitivity of the CMOS rectifier, but strongly depends on the Q of the passive components. A large value for X_n results in a large voltage boost factor, but implies a large impedance for the series inductor. Taking into account its losses due to the series resistance, equation (1) is revised to:

$$V_{in} \approx \frac{X_n}{R_n + R_{loss} + R_{ant}} V_{RF} \tag{2}$$

where $R_{loss} = {}^{X_n}/_{Q}$ and Q is the quality factor of the inductor. The relatively large value of the reactance of the inductor (X_n) and its losses (R_{loss}) results in a decrease of the voltage boost factor.

III. High-Q MEMS Resonator

A good replacement to the series inductor used for voltage boosting, Section II, is a high Q 2-port piezoelectric laterally-vibrating MEMS resonator [7, 8]; which can be integrated with a CMOS process [6]. This device is based on a piezoelectric plate sandwiched between two patterned metal layers that are employed to create an electric field across the thickness of the piezoelectric film (H), Fig. 2. The top Al layer is formed by an array of interdigitated electrodes that are alternatively connected to the input (V_{in}) and output (V_{out}) ports while the bottom metal, Mo, is a common ground plate.

The MEMS resonator, vibrating in width-extensional mode, can be modeled in the electrical domain. Fig. 3(a) shows the resonator modeled with parasitic capacitance (C_0) that accounts for the dielectric polarization of the piezoelectric layer, and shows the electrical representation (mBVD model) of a 2-port piezoelectric transducer with 2 input fingers $(n_{in} = 2)$ and 1 output finger $(n_{out} = 1)$ used in place of an inductor, Fig. 1(b). The equivalent stiffness, damping, and mass of each resonator finger are represented by the capacitance (C_m), resistance (R_m), and inductance (L_m). These variables can be determined via 3D Finite Element Analysis of the resonator with the assumption that anchor losses are the primary source of dissipation [9]. Despite the adverse effect of C_0 on the voltage boosting circuit the overall performance is significantly better than inductors.

IV. Rectifier Circuit Design

The voltage conversion gain of the rectifier increases linearly by increasing the number of stages (N) [5]:

$$V_{out,DC} = \frac{N \cdot V_{in}^2}{2V_T} \tag{3}$$

This also increases the input capacitance of the rectifier $(C_n = NC_1)$, in which C_n is proportional to the capacitance of a single stage rectifier (C_1) as additional stages are considered to be in parallel.

$$\left|\frac{V_{in}}{V_{RF}}\right| = \frac{1}{\omega(R_{ant} + R'_m)(C_0 + C_n)} \tag{4}$$

and placing (4) into (3), it becomes:

$$V_{out,DC} = \frac{N \cdot V_{RF}^2}{2V_T\omega^2(R_{ant} + R'_m)^2(C_0 + C_n)^2} \tag{5}$$

To find the optimum number of stages, take the derivative of (5) and set it to zero:

$$\frac{\partial V_{out,DC}}{\partial N} = 0 \Rightarrow \frac{(C_0 + C_n) - 2C_n}{(C_0 + C_n)^3} = 0 \tag{6}$$

Which results in optimum N given by

$$N_{opt} = \frac{C_0}{C_1} \tag{7}$$

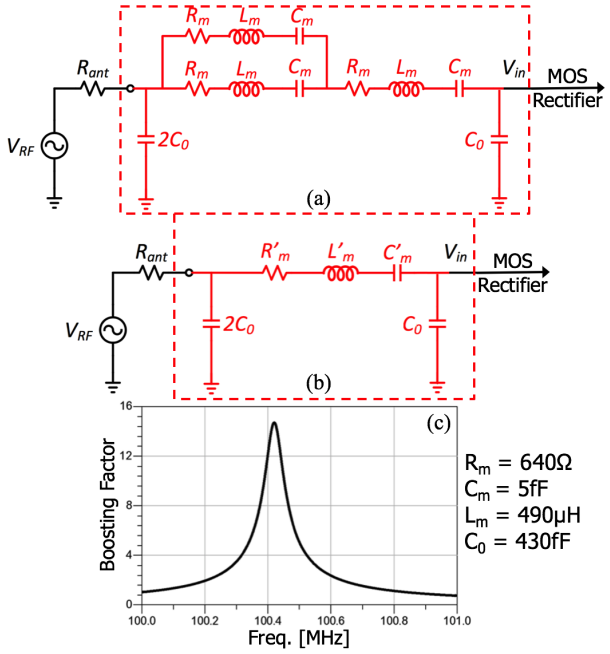

Fig. 3: (a) The Butterworth Van-Dike (mBVD) circuit model for the high-Q piezoelectric resonators, (b) a simplified model for the piezoelectric resonators, (c) typical voltage boosting factor versus frequency.

V. Low-Power Comparator

A nano-watt fully differential comparator (Table I), used to sense the change in rectifier output voltage (Fig. 1), has been configured in negative feedback to null the DC offset due to mismatch and the steady-state rectifier output (Fig. 4). Once nulled, the comparator's output will produce a high-jitter oscillation closer to half the frequency of the clock. If the change in voltage from the rectifier is less than the slope I/C, the integrator slew rate, the resulting output from the comparator oscillates, otherwise it will stop until the integrator (REF) has caught up (Fig. 5). This circuit can detect signals bounded in the frequency range of $I/(2\pi CA) < f_{sig} < f_{clk}/2$, where A is the amplitude of the received equivalent sinusoid.

The NMOS input pair of the StrongARM latch operates in the subthreshold region for additional power savings. The cross-coupled PMOS provides very high gain with long enough sample time due to positive feedback (Fig. 6 (a)). The outputs of the StrongARM latch are connected to a set of inverters to provide additional gain (Fig. 6 (b)) to create digital decisions, and to generate logic lows during reset to hold the SR-latch

TABLE I: Simulated Comparator Power [nW]

0.5 V Comparator				**±0.5 V I/Os**		
Comp. Core*	Clock Gen.	Current Anlg†	Dig.‡	Level Shifter	Pattern Detect	Other⋆
5.5	0.27	0.16	0.16	1.9	10.8	147

∗StrongArm latch, SR-latch, and 19 inverters
†Widlar current source and ‡ isolation mirrors
⋆Higher power buffers for testing, programing, and redundancy with a input chopper circuits

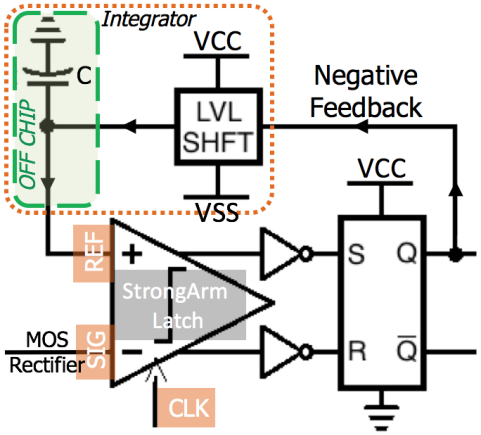

Fig. 4: The block diagram of the nano-watt comparator including a StrongARM latch, Switched-Current Source Push-Pull (SCSPP) inverters (Fig. 6 (b)), SCSPP SR-latch, and SCSPP level shifter used as an integrator.

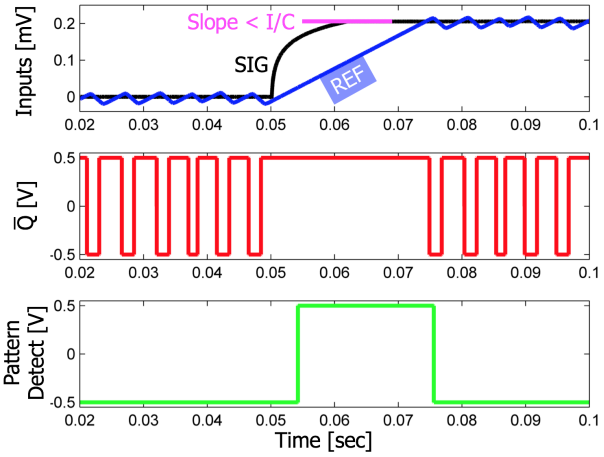

Fig. 5: Simulated comparator behavior.

(Fig. 4). The SR-latch result is passed into an integrator, level-shifter with capacitor, which is used to generate both positive and negative voltages to eliminate offset (Fig. 4). SCSPP style logic is used for all low-power digital circuits to make fanout, short-circuit current, and switching threshold voltage a function of sizing current

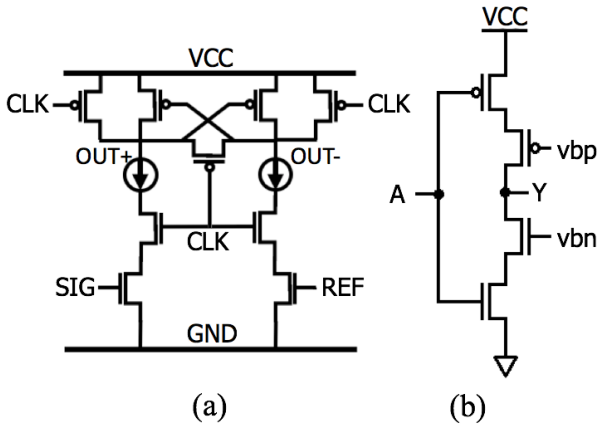

Fig. 6: Modified StrongARM latch schematic [10] (a), and SCSPP logic style inverter (b).

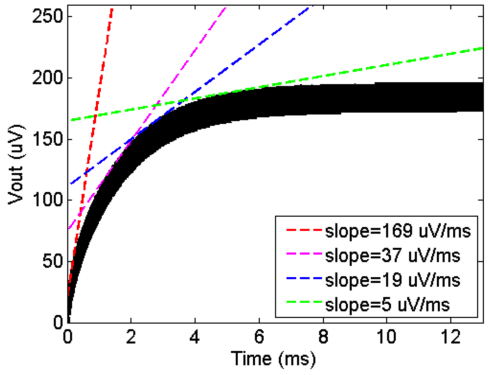

Fig. 7: Simulated output of 5 stage CMOS rectifier, $N_{opt} = 5$, for input signal of -60 dBm.

mirrors while maximizing drive to the load with near rail-to-rail logic.

The equivalent circuit model of Fig. 3 (a) is used to find the optimal number of stages (N_{opt}) as defined in equation (7) for the rectifier circuit in Fig. 1. In Fig. 7, it can be observed that the initial slope of the output of the rectifier is greater than the minimum slope $I/C = 8.95\,\mu\text{V/ms}$ indicating RF signal detection.

VI. Conclusion

A nano-power voltage-boosted WuRx with -60 dBm sensitivity, simulated input of 628 µV, is designed in a 0.13 µm CMOS process using the technique explained above. A piezoelectric resonator with Q of 500 was designed in an AlN process that can be integrated with the nanowatt CMOS comparator at the wafer level. Table II compares the post-layout simulation results of the proof-of-concept prototype circuit with some of the reported low-power wake-up receivers in the literature.

TABLE II: Performance Summary and Comparison

Reference	[1]‡	[2]	[3]	[4]	**WuRx**
Power [µW]	22.9	45	52	65	0.166◇
Sensitivity [dBm]	-75.0	-62.0	-70.0	-48.0	-60.0
Energy [nJ/bit]	0.11	0.14	0.26	0.65	-
Modulation	OOK	FSK	OOK	OOK	SD⋆
Rx Median	RF	BCC†	RF	RF	RF
Freq [GHz]	0.9	0.08	2.0	1.9	0.1
Supply [V]	0.5	0.7	0.5	0.5	±0.5
Tech [nm]	130	180	90	90	Mix∗

⋆Signal detection; ∗IBM 130 nm & InvenSense MEMS
◇Simulated power; †body channel communication
‡Reporting lowest Energy per bit mode

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