Tunable Blocker-Tolerant On-chip Radio Frequency Front-end Filter with Dual Adaptive Transmission Zeros for Software Defined Radio Applications

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***Abstract*— This paper presents a tunable active bandpass filter with adjustable transmission zeros (TZ) close to the passband for software defined radio applications. The RF front-end frequency selectivity is enhanced by the creation of TZs which also improve the out-of-band (OOB) input-referred third-order intercept point (IIP3). The filter is based on two-path signal cancellation and consists of a tunable bandpass filter in parallel with two tunable bandstop filters. This combination ensures the correct amplitude and phase relationships across a wide tuning range to create adjustable TZs without sacrificing the gain of the passband. This paper presents in detail the design considerations and guidelines, as well as analysis of the filter performance in the presence of non-idealities such as parasitics and imperfect clock signal shape. The proposed filter is implemented with high-Q N-path filter blocks in a 65-nm CMOS process. The passband of the filter is tunable from 0.1 GHz to 1.4 GHz with a 3-dB bandwidth of 9.8–10.2 MHz, a gain of 21.5–24 dB, a noise figure of 3–4.2 dB, and a total power consumption of 50–73 mW. TZs are created on both sides of the passband with a minimal offset of 25 MHz and are tunable across a 20 MHz range with up to 60 dB rejection. The measured blocker 1-dB compression point is 8 dBm and the out-of-band IIP3 is 23 dBm. The reported filter provides a promising on-chip filtering solution for multi-standard, multi-frequency software-defined radio applications with improved interference mitigation capabilities.**

***Index Terms*— software radios, active filters, tunable filters, CMOS, Bandpass, N-path, RFIC, transmission zero, switched-capacitor, carrier aggregation.**

I. Introduction

In the face of an increasing demand for high data rate connectivity and the scarcity of the available frequency spectrum, the last two decades have witness the development of many innovations in wireless communication technologies. One example is software defined radios (SDRs) which can adapt their operating parameters, such as frequency and modulation scheme, by field programmability [2]–[4]. A common limitation of SDRs is a lack of high quality programmable/tunable front-end filter, which makes the SDR receiver susceptible to strong interferers from both fixed frequency and other SDR users [5].

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This issue is exacerbated as the wireless communication industry moves to advanced long-time evolution (LTE-A) standards. The plethora of allocated frequency bands opens up demand for SDR based front-end transceivers, and at the same time, highlights the need for low-loss high-selectivity tunable filters. In particular, carrier aggregation (CA) which allows an aggregated higher data rate by simultaneously combining multiple transmit/receiver carriers presents new challenges in frontend filtering. Both intra-band aggregation (RF channels belong to the same band) and inter-band aggregation (different bands) are supported in 3GPP standard [6]. The channels can be adjacent to one another (contiguous) or not (non-contiguous) for intra-band aggregation. Suppressing near-by (in frequency) high power transmit signals (blockers) from either its own or near-by (in location) transmitter is necessary to avoid desensitizing the receiver.

To handle large out-of-band (OOB) blockers, various on-chip techniques, including current-mode architectures [7]–[12] and mixer-first architectures [13], [14], have been reported recently. These techniques translate the baseband low-pass impedance profile to the radio-frequency (RF) carrier frequency and creates an equivalent high-Q bandpass filter (BPF) centered at the local oscillator (LO) frequency. RF BPFs have also been reported based on the similar N-path filtering technique [15]–[18] which can emulate high-Q LC tank with a tunable center frequency and constant bandwidth. Frequency tunable high-Q BPF can be synthesized at the carrier frequency using discrete-time signal processing [19]–[21].

Even though the aforementioned techniques show promise in handling large OOB blockers, the performance may still be insufficient in carrier aggregation scenarios, especially when large blockers are located very close to, or even between, the weak desired RF channels. To this end, BPFs with transmission zeros (TZs) located at the blocker frequency may become a necessary solution [22].

This paper presents novel design techniques to create highly selective on-chip N-path tunable filters with adjustable transmission zeros very close to the passband edges. The central idea is to use multiple signal paths with appropriate gain and phase profiles (with respect to frequency) to create interference cancellation at select frequencies. The major advantage of this strategy is the ability to create close-in TZs, e.g. 25 MHz from a 1-GHz center frequency as demonstrated in this work, with a favorable trade-off in area, power consumption, and out-of-band rejection, than simply increasing the BPF filter order.

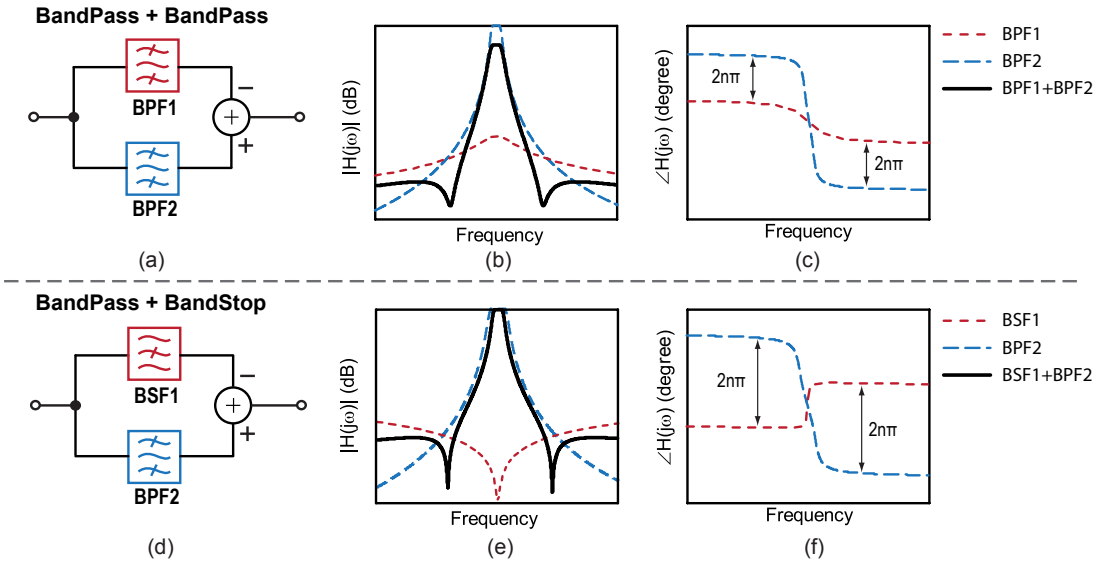

Fig. 1. (a) Two BPF with different amplitude can be used in parallel to create dual transmission zeros on both side [23]. The insertion loss is increased due to the subtraction of two BPFs. (b)&(c) Magnitude and phase response respectively for the case shown in (a). (d) The proposed transmission zero creation concept. A BPF in the main path along with a BSF in the auxiliary path creates two TZs, one on each side of the passband, by judicious choice of the magnitude and phase responses. The insertion is not increased due to the use of the BSF in parallel path. (e)&(f) Magnitude and phase response respectively for the case shown in (d).

It is noted that there has been significant research devoted to developing wideband linear low noise amplifiers (LNA) to ensure co-existence of the weak received signal with strong blockers [22], [24], [25]. Due to smaller supply voltages used in modern CMOS processes and hence the voltage swing limitation at the LNA output, achieving high linearity is still challenging. In addition, due to the power level variations in RF carriers, a shared LNA with a fixed power gain may not present an optimum solution in carrier aggregation scenarios. The proposed filter design in this paper will be a compliment to high linearity LNA designs by providing significant blocker rejection up front. In fact, it has been shown in [26] that incorporating a bandpass filter in front of the LNA improves the linearity significantly. Several tunable duplexers have been demonstrated recently [27], [28] along the same line.

Built upon our previous work [1], this extension paper presents in detail the strategy, considerations, and guidelines for the design of the proposed tunable filter. Besides presenting detailed linearity and noise analysis, we also investigate the impact of non-idealities, such as parasitics and finite switching time, on the filter performance. Finally, the implementation details and measured results of the proposed filter are presented.

II. Transmission Zero Creation Mechanism

Creating TZs near the passband has been a popular strategy in passive high frequency filter designs to improve the rejection of close-in interferers (blockers) [29]. More recently, this idea has also been investigated for active filter designs.

Feed-forward techniques [30]–[34] or cascading of a bandpass filter (BPF) and a bandstop filter (BSF) with different center frequency [35]–[37] have been proposed to suppress transmit (TX) leakage and TX noise in the receive band. In [22], a TZ is created on one side of the passband by using a BPF+BSF cascade in the feedback path. A second TZ can also be obtained by adjusting the clock bias voltage. However, in these architectures, the bandwidth (BW) and TZ position are coupled with each other. The passband gain and noise figure degrade significantly if the TZs are placed close by. For example, in [22], the closest TZ is ∼250 MHz offset from the passband, which is insufficient for CA applications.

A second school of thought is to split the signal into multiple paths and achieve out-of-phase cancellation at select frequencies. For two signals at the same frequency, the criteria is that the two signals should have the same magnitude but differ in phase by an odd multiple of π. This simple idea forms the basis for TZ creation in cross-coupled passive resonator filters [38], and has also given rise to signal-interference type microwave filters [39]–[41].

Along this line, it has been proposed that two tunable bandpass filters with different amplitudes can be subtracted to create two TZs beside the passband [23]. However, the insertion loss degrades due to the subtraction of the two filter gains as illustrated in Fig. 1(a)[1]. Following our previous ideas [1], [42], we propose a novel and more effective TZ creation strategy by combining a tunable bandpass filter in parallel with a tunable bandstop filter to satisfy the correct magnitude and phase relationships for the creation of TZs close to the passband (Fig. 1(b)). The choice of using a bandstop filter in the auxiliary path is based on two main considerations. First, the use of two filters ensures that the correct phase relationship can be met over a wide frequency tuning range as both filters could be tuned synchronously. Second, due to the use of the bandstop filter in the parallel path, the passband gain is not reduced when the signals from the two paths are subtracted.

As a vehicle to illustrate the proposed concept, a simple

[1]Fig. 1(a) is a conceptual rendering rather than an exact reproduction of the design concept in [23]

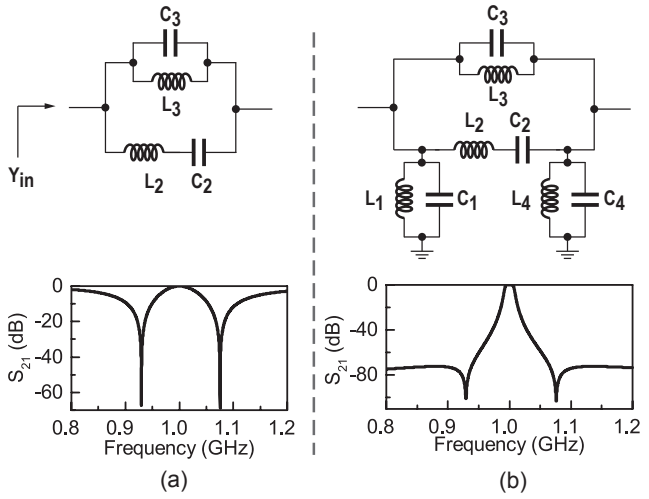

Fig. 2. (a) Two TZs can be created by putting a 2^{nd}-order bandstop filter in parallel with a 2^{nd}-order bandpass section. The cancellation of the pole by the TZ renders the out-of-band rejection unusable as a practical filter. (b) A 6^{th}-order bandpass filter in parallel with a 2^{nd}-order bandstop filter is shown here to create similar close-in TZs as in (a).

static passive filter circuit shown in Fig. 2(a) is first analyzed. A parallel LC section (bandstop) is connected in parallel with a series LC section (bandpass). The circuit creates two TZs, one on each side of the passband as shown in Fig. 2(a).

The input admittance Y_{in} is given by

$$Y_{in} = \frac{1 + s^2\left(L_2C_2 + L_3C_3 + L_3C_2\right) + s^4 L_2C_2L_3C_3}{sL_3(1 + s^2L_2C_2)}. \quad (1)$$

By setting the numerator of $Y_{in} = 0$, the two TZ frequencies can be obtained as

$$\omega^2_{\text{notch}} = \frac{k \pm \sqrt{k^2 - 4L_2C_2L_3C_3}}{2L_2C_2L_3C_3}, \quad (2)$$

where $k = L_2C_2 + L_3C_3 + L_3C_2$. Using L_2 =200 nH, C_2 =0.13 pF, L_3 =4.3 nH and C_3 =5.9 pF, the TZ frequency is calculated as 922.3 MHz and 1.07 GHz, which matches exactly with simulation as shown in Fig. 2(a).

A drawback of this circuit is that, due to the cancellation of the poles by the zeros, the ultimate out-of-band rejection is very low. To overcome this problem, a higher order (6^{th}) bandpass filter can be used instead (Fig. 2(b)). This configuration maintains the TZs at the same position and the ultimate rejection is better compared with that of Fig. 2(a). In the simulation, $L_1 = L_4 = 20\,\text{pH}$, $C_1 = C_4 = 1.27\,\text{nF}$ and $L_2 = 200\,\text{nH}$, $C_2 = 0.13\,\text{pF}$, $L_3 = 4.3\,\text{nH}$, and $C_3 = 5.9\,\text{pF}$ with terminations of $50\,\Omega$. A similar concept is also shown recently in [43] to create high-Q bandpass filters with quasi-elliptic frequency response using acoustic wave lumped element resonators. However, as shown in Fig. 2(a), the out of band rejection is poor due to the cancellation of poles.

To improve the out of band rejection and create the TZs, the difference in the number of resonators between the bandpass and bandstop filters should be $2n$, where $n = 0, 1, 2, ...$ to fulfill the phase requirement.

III. Proposed Filter Design

In this section, we will describe the initial design of the proposed filter. The design follows the 6^{th}-order-BPF + 2^{nd}-order BSF from Fig. 2(b). Parallel LC tanks can be replaced by their N-path counterparts. The series LC tank ($L_2\&C_2$) in Fig. 2(b) can be transformed into a shunt parallel LC tank by two impedance inverters represented by the "J" blocks as shown in Fig. 3(a). The impedance inverters can be implemented with active gyrators formed by back-to-back g_m cells [17] as shown in Fig. 3(b). A network connected to one port of a gyrator is seen as its dual network in the second port. The active gyrator ensures that the impedance inverting property can be realized over a wide frequency tuning range.

The grounded LC resonators can be implemented with shunt configuration of N-path filters [16] and the floating bandstop resonator can be implemented with series configuration of N-path filters [44] as shown in Fig. 3(c&d).

Assuming the same bandwidth for the RLC resonator and the N-path switched capacitor resonator, the corresponding R_B, C_B and L_B values for the N-path bandpass filter and R_N, C_N and L_N values for the N-path bandstop filter can be obtained using state space analysis [16], [36] as follows,

$$R_B = \frac{N\left[1 - \cos(2\pi D)\right]R_s + 2D\pi^2\left[R_s(1 - ND) + 2R_{sw}\right]}{2N(D\pi)^2 - N\left[1 - \cos(2\pi D)\right]}, \quad (3)$$

$$C_B = C_{BB}\frac{ND\pi^2}{m[N\sin^2(\pi D)] + D\pi^2(1 - ND)}, \quad (4)$$

$$L_B = \frac{1}{(2\pi f_s)^2 C_{BB}}, \quad (5)$$

$$R_N = R_T\frac{N\sin^2(\pi D) + D\pi^2(1 - ND)}{N\left[(\pi D)^2 - \sin^2(\pi D)\right]}, \quad (6)$$

$$C_N = C_{NN}\frac{ND\pi^2}{m[(N\sin^2(\pi D)] + D\pi^2(1 - ND)}, \quad (7)$$

$$L_N = \frac{1}{(2\pi f_s)^2 C_N}, \quad (8)$$

where $R_T = R_s + R_{swN} + R_L$, D is the duty cycle of the clock and $m = 2$ for single-ended circuits and $m = 8$ for the differential circuits [44].

To increase the gain, reduce the noise figure (NF), and increase the dynamic range of the filter, the first gyrator is replaced with a single g_m cell (amplifier) [17]. This effectively transforms the 6^{th}-order (3-pole) bandpass filter prototype to a cascade of a 2^{nd}-order (1-pole) filter with a 4^{th}-order (2-pole) filter. The OOB roll-off of the BPF still follows a 3-pole characteristic due to the impedance isolation by g_{m1}.

A differential configuration is exploited for the filter design. The g_m cells are implemented with self-biased inverters except g_{m4} as shown in Fig. 4(b). A current starving self-biased inverter is used for g_{m4} to control the g_m, which is necessary for better matching of the two paths to create TZs. Two negative resistors made of back-to-back inverters are added after the second and third BP resonators to increase the quality factor (Q) of the resonators. These negative resistors have a separate supply voltage (V_{DD1}) with a nominal value of

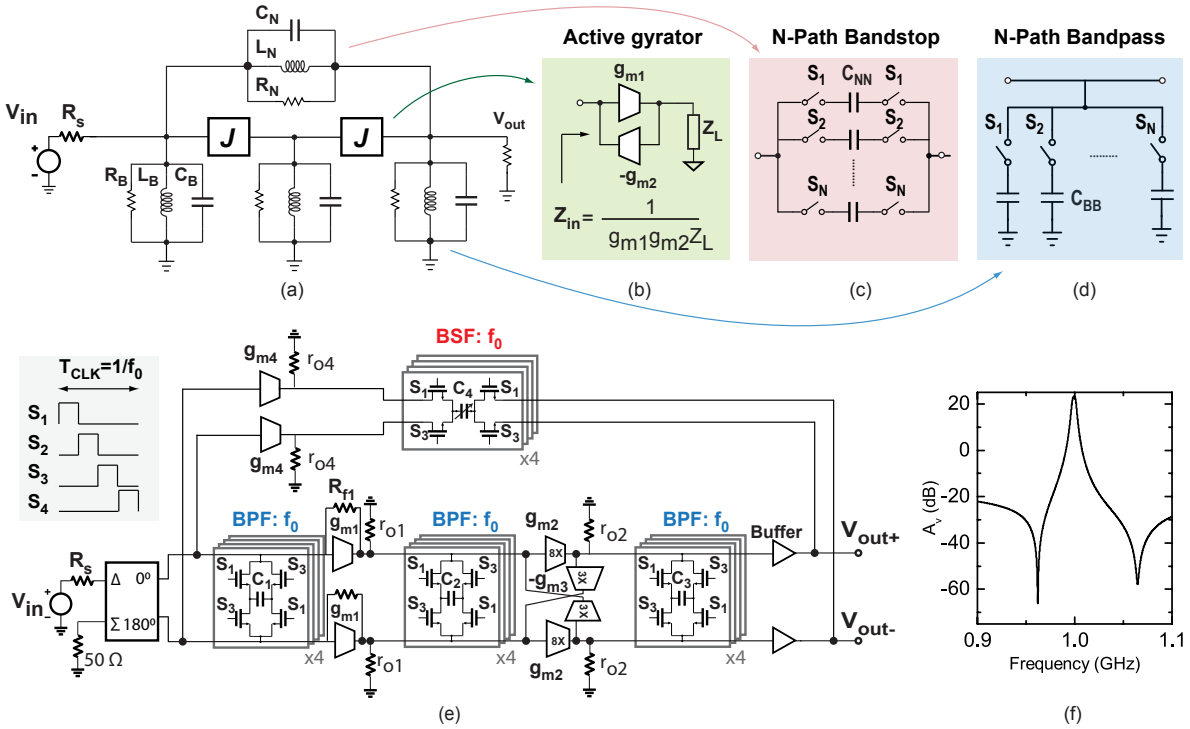

Fig. 3. First iteration design of the proposed tunable filter with adjustable dual TZs. (a) Passive filter prototype; (b) Implementation of the impedance inverters by back-to-back g_m cells. (c) Implementation of the bandstop resonator by series-connected N-path filter; (d) Implementation of the bandpass resonators by shunt-connected N-path filter; (e) Schematic diagram of the proposed filter; (f) An example simulated frequency response at 1 GHz showing a high filter shape factor and deep TZs on both sides of the passband.

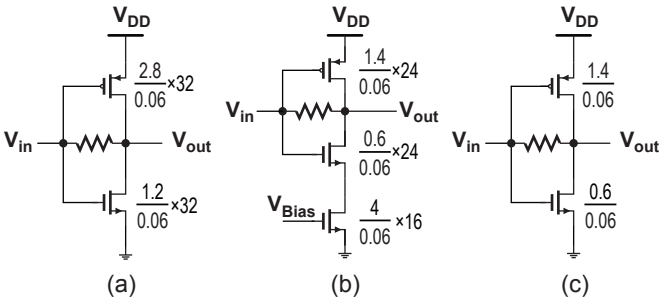

Fig. 4. (a) The g_{m1} cell; (b) The g_{m4} cell; (c) The unit g_m cell that is used in the filter with different scaling factors (g_{m2}, g_{m3}).

1.2 V. However, large amount of negative admittance reduces the dynamic range (DR) as well as reduces the linearity and also increases the power dissipation. To make the gyrator stable, two diode connected inverters are added at the output of the filter to provide common mode feedback. To increase the gain and to reduce the noise, g_{m2} is made bigger than g_{m3}. The various g_m values, output impedance r_o values, and the baseband capacitor C_{BB} value are listed in Table I. The filter is capable of frequency tuning by changing the LO frequency. A snapshot of the simulated frequency response of the filter at 1 GHz (Fig. 3(f)) shows a high filter shape factor and two close-in (-40 MHz & 65 MHz) TZs with high rejection (>80 dB with respect to the passband gain).

The input impedance of the receiver, Z_{in} is defined as the ratio of the fundamental components of voltage and current at the input port. Following the procedure in [11], Z_{in} of the filter at the resonant frequency f_s can be found as

$$Z_{in}(\omega) \simeq \Big\{ R_{sw} + \frac{N}{\pi^2} \sin^2\left(\frac{\pi}{N}\right) \times [Z_{BB}(\omega - \omega_{LO}) + Z_{BB}(\omega + \omega_{LO})] \Big\} || \frac{R_{f1}}{1 + g_{m1} r_{o1}}, \quad (9)$$

where N is the number of clock phases and Z_{BB} is the impedance of baseband capacitor C_{BB}. The values of R_{f1} (4.6 kΩ) and g_{m1} (77.58 mS) are chosen properly for input impedance matching.

TABLE I
DESIGN PARAMETERS

g_{m1}	77.58 m	C_1	34 pF	r_{o1}	106 Ω
g_{m2}	10.23 m	C_2	45 pF	r_{o2}	592 Ω
g_{m3}	3.85 m	C_3	45 pF	-	-
g_{m4}	27.58 m	C_4	1.13 pF	r_{o4}	312 Ω
g_{m5}	24.87 m	C_5	1.04 pF	r_{o5}	243.3 Ω

IV. Linearity Analysis

In this section, we will analyze the benefits of creating TZs in terms of linearity. To determine the receiver input-referred third-order intercept point (IIP3), the level of in-band third-order intermodulation products (IM3) of any two blockers should be investigated. For two blockers with frequency of f_{BLK1} and f_{BLK2} (Fig. 5), the in-band IM3 product is

$$f_{RX} = 2f_{BLK1} - f_{BLK2}, \quad (10)$$

and the other term $2f_{BLK2}-f_{BLK1}$ falls outside of the receive (RX) band.

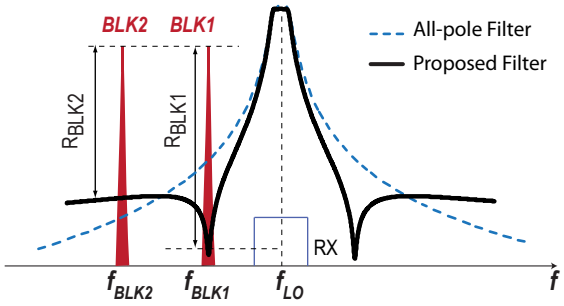

Fig. 5. Comparison between proposed filter and an all pole filter with respect to linearity in presence of blockers.

The output of a system can be modelled as $y(t) = \alpha_1 x(t) + \alpha_2 x(t)^2 + \alpha_3 x(t)^3$, where the input is $x(t)$. If two sinusoidal signals with amplitude A_1 and A_2 are applied to the system, the resulting IM3 and IIP3 are [45]

$$A_{IM3} = \frac{3}{4} \times \alpha_3 A_1^2 A_2 = \frac{\alpha_1}{A_{IIP3}^2} A_1^2 A_2,$$

and

$$A_{IIP3} = \sqrt{\frac{4}{3}\left|\frac{\alpha_1}{\alpha_3}\right|},$$

where A_1 and A_2 represents the amplitude of two blockers.

The IIP3 of the entire receiver unit can be found as follows

$$P_{IIP3-RX}(dBm) = P_{BLK}(dBm) + \frac{P_{BLK}(dBm) - [P_{IM3,out}(dBm) - A_{v-Rx}(dB)]}{2}, \quad (11)$$

where P_{BLK} is the blocker power level, A_{v-Rx} is the gain of the entire filter. The filter provides different rejections, R_{BLK1} and R_{BLK2} for the two blockers at f_{BLK1} and f_{BLK2} respectively. Fig. 5 shows the filtering behavior for the proposed filter and an all pole filter in the presence of two blockers. The IM3 level at the filter output is given by [26].

$$A_{IM3} = \frac{A_{v-RX}}{R_{BLK1}^2 R_{BLK2}} \frac{A_1^2 A_2}{A_{IIP3}^2}. \quad (12)$$

The goal is to make the A_{IM3} smaller to increase the overall IIP3. The overall IIP3 improvement is

$$\uparrow P_{IIP3-RX}(dB) = R_{BLK1}(dB) + \frac{R_{BLK2}(dB)}{2}. \quad (13)$$

The improvement in linearity by adding the TZ can be seen by comparing the proposed filter with an all-pole filter with the same order and similar gain. As an example, if the proposed filter provides 15-dB extra attenuation at f_{BLK1} and 8-dB worse attenuation compared to an all pole filter at f_{BLK2}, then according to (13), the IIP3 improvement is 11 dB. As a result, the proposed filter provides better linearity compared with an all pole filter with similar gain.

V. Non-ideal Effects

A. Parasitic Capacitance

Due to the parasitic capacitance at different nodes of the filter, the expected dual-TZ behavior cannot be achieved as shown in the post-layout simulation (Fig. 6) of the proposed filter structure (Fig. 3(e)).

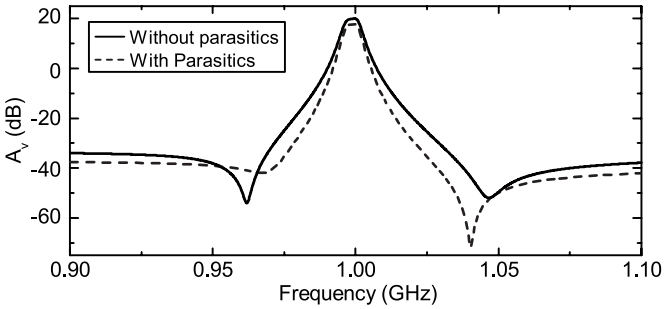

Fig. 6. Effect (simulation) of parasitics on the filter frequency response, particularly the TZ rejection level. Although the plot is created at 1 GHz, the effect is similar at other frequencies.

In this section we will analyze the parasitic capacitance effect on both the bandpass and bandstop filters. Even though the effect of parasitic capacitance on bandpass N-path filters has been analyzed in [17], the resulting expressions do not provide much design insight due to their complexity. In this paper, we will analyze the parasitic capacitance effect for both bandpass and bandstop resonators using a passive RLC resonator as an equivalent circuit. Fig. 7(a&b) show the RLC and N-path bandpass and bandstop resonators with parasitic capacitances (C_P, C_S, and C_L).

The transfer function for the grounded LC resonator with input parasitic capacitance C_p is

$$H_{BP}(s) = \frac{s^2 L_B C_B R_B R_{SWB} + sL_B(R_B + R_{SWB}) + K}{T(s)}, \quad (14)$$

where $K = R_B R_{SWB}$ and

$$\begin{aligned} T(s) =& s^3 L_B C_B C_P R_S R_B R_{SWB} + s^2 [L_B C_B R_B (R_s \\ &+ R_{SWB}) + L_B C_P R_s (R_B + R_{SWB})] \\ &+ s[L_B(R_B + R_{SWB}) + C_P R_s R_B R_{SWB} + L_B R_s] \\ &+ R_B(R_s + R_{SWB}). \end{aligned} \quad (15)$$

Assuming the switch on resistance R_{SWN} is small in Fig. 7(b), the transfer function for the floating LC resonator with source and load parasitic capacitance C_s and C_L can be found as

$$H_{BS}(s) = \frac{s^2 L_N C_N R_N R_L + sL_N R_L + R_N R_L}{T_1(s)}, \quad (16)$$

and

$$\begin{aligned} T_1(s) =& s^3 L_N R_N R_s R_L [C_L(C_N + C_s) + C_s C_N] \\ &+ s^2 L_N [C_L R_L (R_s + R_N) + R_s R_N (C_s + C_N) \\ &+ C_N R_N R_L + C_s R_s R_L] \\ &+ s[R_s R_N R_L (C_s + C_L) + L_N (R_N + R_s + R_L)] \\ &+ R_N (R_s + R_L). \end{aligned} \quad (17)$$

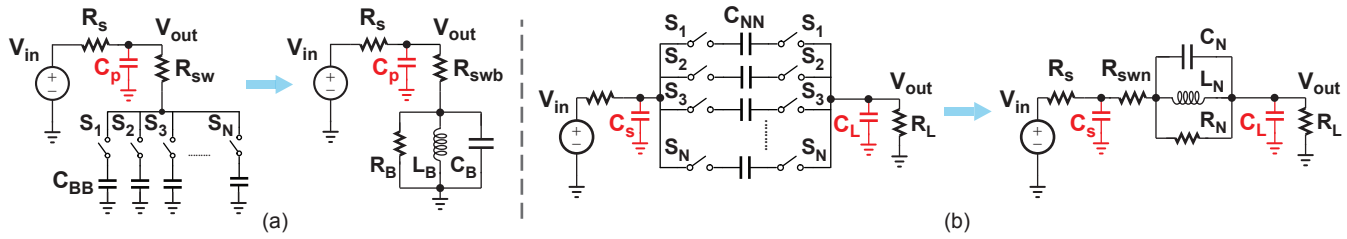

Fig. 7. Equivalent parasitic capacitance at input and output nodes of the (a) bandpass and (b) bandstop filter.

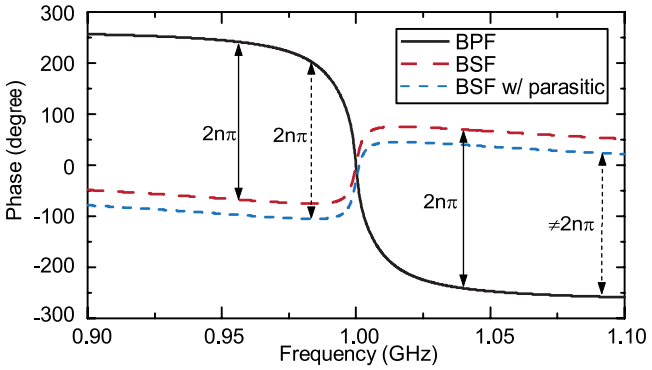

Fig. 8. Symmetric phase responses for both the bandpass and bandstop filters create dual TZs on both sides of the passband (simulation). However, a shifted phase response of the bandstop filter creates a single TZ.

From (16), we can find the frequency shifting of the bandpass resonator due to C_P

$$\omega_{new,BP} = \omega_{LO} - \frac{\omega_{LO} \times C_P R_s}{2C_B R_B} \times \frac{R_B + R_{SWB}}{R_s + R_{SWB}}. \quad (18)$$

Similarly, the frequency shifting of the bandstop (BS) resonator can be obtained as

$$\omega_{new,BS} = \omega_{LO} - \frac{\omega_{LO} \times (R_L \times (C_L R_N) + C_S R_s) + R_s R_N C_S}{2C_N R_N (R_s + R_L)}. \quad (19)$$

The parasitic capacitance for the bandstop filter include contributions from the top side of the switches, RF signal routing line, top and bottom plates of the metal-insulator-metal (MIM) capacitors, and the input capacitance of the main signal path. As a result, there is crosstalk among the 4 clock paths since C_P is interacting with $C_1 - C_4$ during each clock phase. Fig. 9(a&c) show the simulated and theoretical behavior (14) for the bandpass resonator with parasitic capacitance. Here we assume R_s =50 Ω, C_B =121.8 pF, $C_{BB} = 4/\pi^2 \times C_B$ =49.3 pF, C_N =3 pF, R_{sw} =10 Ω and R_L =1 kΩ. Due to the impact of C_P, the center frequency decreases slightly as shown in Fig. 9(a) and the insertion loss increases due to crosstalk.

In contrast to the bandpass filter, the center frequency of the bandstop filter does not change much (Fig. 9). The baseband capacitor for the BS is small (1.13 pF) in our proposed filter implementation. However, both the magnitude and phase response show asymmetric behavior due to the parasitic capacitance as shown in Fig. 9(b&d).

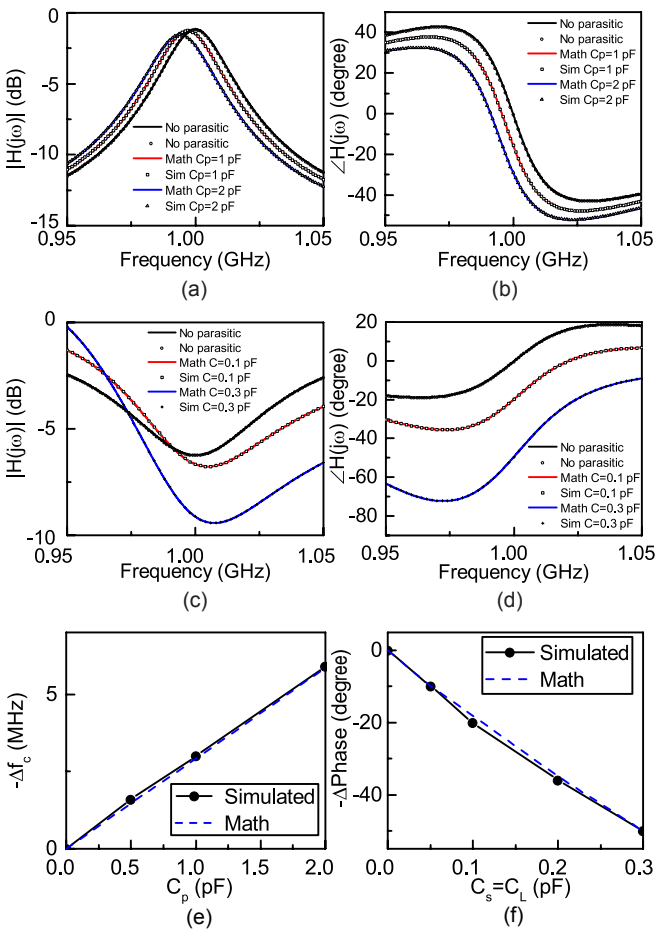

Fig. 9. Simulated and modeled (a&c) magnitude and (b&d) phase responses of bandpass and bandstop filters with different parasitics. (e) Simulated center frequency shifting of bandpass filter due to parasitics. (f) Simulated phase shifting of bandstop filter at the center frequency due to parasitics.

Parasitic-induced phase shifting of the bandstop filter is shown in Fig. 9(f). Due to the phase asymmetry, it is difficult to generate two TZs as the phase requirement does not fulfill simultaneously on both sides of the passband (Fig. 8). Section. VI-A will discuss techniques to overcome this problem.

B. Clock Duty Cycle

In this section, we will consider the clock duty cycle effect. The finite rise and fall time are considered as part of the overall duty cycle reduction (Fig. 10).

To find the transfer function $H_{tot}(s)$ of the filter, the switches and capacitors are substituted with an equivalent

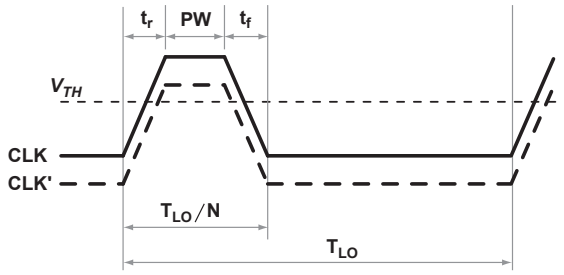

Fig. 10. Clock waveform with finite rise and fall time used in the analysis. The clock signal (CLK) is ideally biased at the threshold voltage of the switches. Changing the clock bias, as indicated by the CLK' signal, can be used as a method to adjust the duty cycle.

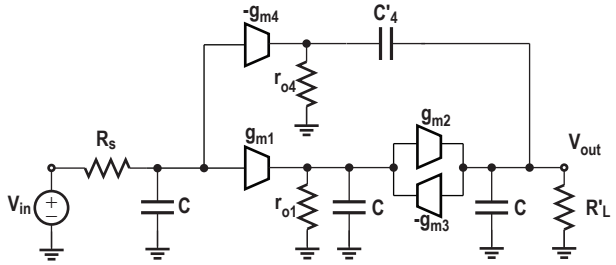

Fig. 11. The low-pass equivalent circuit of the filter in Fig. 3(e).

baseband capacitor of C_{BB}/D. After that we find the transfer function $H_{LPF}(s)$ of the baseband equivalent circuit. Then, we translate $H_{LPF}(s)$ in frequency to ω_{LO} and multiply the resulting transfer function by $\text{sinc}^2(\pi/D)$ [16], [17], where D is the effective duty cycle of the clock. The effective duty cycle $D = PW + (t_r + t_f)/2$ because the switches are turned on halfway in both the clock rise and fall times.

According to the principle mentioned earlier, Fig. 11 is used to find the transfer function of the corresponding baseband structure. Assuming $C = C_1/D = C_2/D = C_3/D$, $C'_4 = C_4/D$ and $R'_L = R_L \| r_{o2}$, we find

$$H_{LPF}(s) = \frac{N(s)}{M(s)}, \tag{20}$$

where

$$N(s) = s^2 C C'_4 g_{m4} r_{o1} r_{o4} R'_L + sC r_{o4} R'_L (g_{m1} g_{m2} r_{o1} + g_{m4}) + g_{m1} g_{m2} r_{o1} R'_L,$$

$$M(s) = (1 + sCR_s)\left[s^3 C^2 C'_4 r_{o1} r_{o4} R'_L + s^2 C\left(CR'_L r_{o1} + C'_4 k'\right) + s\left(CR'_L + C'_4 g_{m2} g_{m3} r_{o1} r_{o4} R'_L\right) + g_{m2} g_{m3} r_{o1} R'_L + 1\right],$$

and

$$k' = r_{o1} R'_L + r_{o1} r_{o4} + R'_L r_{o4}.$$

Therefore

$$H_{tot}(s) = ND \times \text{sinc}^2\left(\frac{\pi}{D}\right) \times [H_{LPF}(s - j\omega_{LO})] + (1 - ND) \times H_{DC}, \tag{21}$$

where $H_{DC} \approx g_{m1}/g_{m3}$ is the transfer function without the baseband capacitors in Fig. 11.

The effect of the clock duty cycle on the proposed filter is shown in Fig. 12. If the duty cycle of the clock D is smaller than $1/N$, all switches are periodically OFF for some time in each cycle and the output signal of the N-path filter tracks the input signal, resulting in higher input impedance for frequencies far away from the switching frequency and its odd harmonics, which then translates to less OOB rejection [35]. On the other hand, if $D > (1/N)$, two switches will be ON at the same time, which results in undesired charge sharing between capacitors and hence a degradation of the insertion loss. Careful layout is necessary to ensure D close to $1/N$ and to increase the matching between different clock phases.

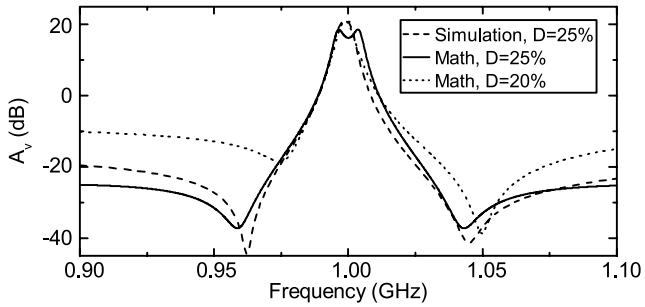

Fig. 12. Effect (simulated) of duty cycle on filter frequency response. Although the plot is created at 1 GHz, the effect is similar at other frequencies.

The simplified block diagram of quadrature clock generator is shown in Fig. 13 [46]. A master clock (CLK) at 4 times the switching frequency is applied from off-chip. A D-flip-flop (D-FF) based divider divides the input clock by 4 while an AND gate between node X and Y generates a 25% duty cycle clock. The output of the D-FFs ($Q_1 \sim Q_4$) and a delayed version of the output are sent to the AND gates to produce 4-phase clocks ($S_1 \sim S_4$) with reduced clock overlapping. Due to the ANDing of two outputs, the clock duty cycle will be slightly lower than 1/N, which can be compensated by slight tuning of the clock bias voltage V_{CLK}. To reduce even-order harmonics, a differential clocking scheme is utilized. It is important to carefully draw the layout of the clock generation circuitry to ensure good phase matching between the different paths.

VI. Improved Architecture

A. Dual-TZ Creation Strategy

As mentioned above in Section V-A, it is difficult to simultaneously control the TZs on both sides of the passband due to the parasitics. The TZ on one side of the passband can be made deeper but at the penalty of a shallower TZ on the other side (Fig. 6). To overcome this problem, a second BS section is added to give us more degrees of freedom in adjusting the frequency responses of the two signal paths. This addition can be justified in terms of circuit area because the bandstop resonators are purposefully designed to have a larger bandwidth, and therefore uses much smaller capacitors. To avoid mutual interaction between two BS sections, the second BS section is connected before the output buffer. Putting a buffer after second BSF make the performance slightly better,

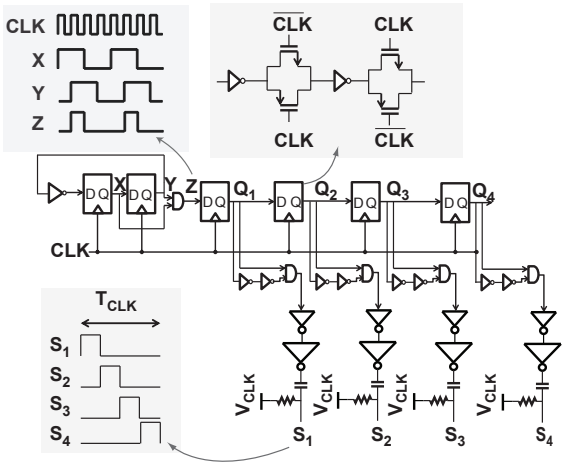

Fig. 13. The clock generation circuitry, adapted from [46].

however there is associated power dissipation with the buffers. Without the buffer, the phase response is still acceptable and two notches can still be generated.

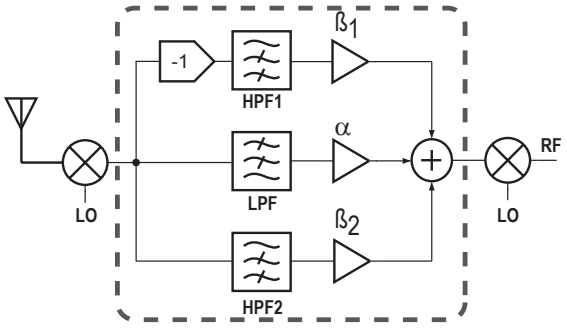

Fig. 14. Concept of dual TZ creation using two BSF paths. BPF and BSFs are modelled with LPF and HPF respectively in the baseband.

It is well known that in a N-path filter, the input signal experiences down-conversion along with low-pass filtering passing through the switches to the capacitors and the same switches up-convert the filtered capacitor voltages to the output node [16]. As a result, it is possible to analyze the corresponding baseband version of the filter with a second high pass filter as shown in Fig. 14. The LPF is considered as a single pole for simplicity. The transfer function of the filter can be written as

$$H(j\omega) = \frac{\alpha}{1+\frac{j\omega}{P_1}} + \frac{\beta_1 \frac{j\omega}{P_2}}{1+\frac{j\omega}{P_2}} + \frac{\beta_2 \frac{j\omega}{P_3}}{1+\frac{j\omega}{P_3}} e^{j\pi}, \qquad (22)$$

where P_1, P_2 and P_3 are the poles of low pass filter (LPF) and high pass filters (HPF) respectively. To create TZ at a particular frequency, the real part and the imaginary part of the numerator of (22) should be zero at that particular frequency. However, this condition can be accomplished by multiple different gain ($\alpha, \beta 1$ and $\beta 2$) and pole (P_1, P_2 and P_3) locations. For example, one possible solution is to set the LPF gain as

$$\alpha = \frac{-X \pm \sqrt{X^2 - 4P_1(P_2+P_3)Y}}{2P_1(P_2+P_3)}, \qquad (23)$$

where $X = \beta_1(P_3^2+2P_1P_3+P_1P_2) - \beta_2(P_2^2+2P_1P_2+P_1P_3)$ and $Y = \beta_1^2 P_3(P_1+P_3) - \beta_1\beta_2(P_1P_2+2P_2P_3+P_1P_3) + \beta_2^2 P_2(P_1+P_2)$.

To obtain a positive α (which is necessary for real frequency TZ creation) two condition need to be fulfilled, either i) $X<0$ and $\sqrt{X^2-4P_1(P_2+P_3)Y} > 0$; or ii) $X>0$ and $Y<0$. However, there are many possible choices to fulfil the criteria. Assuming $\beta_1 > \beta_2$, the TZ frequency can be chosen

$$\omega_{TZ} = \pm\sqrt{\frac{\alpha P_1P_2P_3}{\alpha P_1 + \beta_1(P_1+P_3) - \beta_2(P_1+P_2)}}. \qquad (24)$$

As an example, if we choose $\alpha = 20, \beta_1 = 10, \beta_2 = 8, P_1$ =10 MHz, P_2 = 20 MHz and P_3 = 15 MHz, then according to (29), two TZ frequencies will be ±17 MHz. After up-conversion to f_{LO} =1 GHz, the two TZ frequencies will be 1,017 MHz and 983 MHz. The simulated filter responses with one and two bandstop paths are compared in Fig. 15.

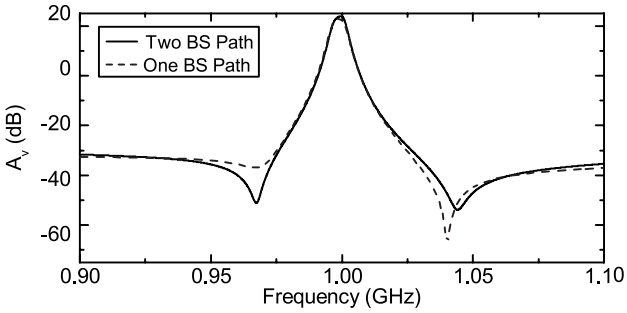

Fig. 15. Simulated filter performance with one and two parallel BS paths including parasitics.

We plot the magnitude and phase responses of BP+1BS filter with or without parasitics along with BP+2BS filter with parasitics in Fig. 16. Adding an extra BS section helps to maintain the symmetric phase at some particular frequencies and dual TZs can still be obtained. In the BP+2BS configuration, it is always possible to create sharp TZs on both sides of the passband, suitable for the desired application of suppressing strong blockers close to the desired channel. The g_m values used in the simulation are g_{ma} = 27.58 mS, g_{mb} = 29.36 mS, g_{mc} = 24.5 mS and C_p = 40 fF, C_{p1} = 20 fF. The Q of the tank is specified as 35.

B. Improved Filter Design

The schematic of the improved tunable filter with dual TZs is shown in Fig. 18. By setting $s=0$ and $D=1/N$ in (20), the center frequency gain of the filter can be found

$$A_v = \frac{g_{m1}g_{m2}r_{o1}R_L'}{1+g_{m2}g_{m3}r_{o1}R_L'} \text{sinc}^2\left(\frac{\pi}{4}\right). \qquad (25)$$

To increase the gain of the filter, g_{m1} needs to be increased and g_{m3} needs to be reduced. However, increasing g_{m1} increases the power consumption and reduces IIP3. Reducing

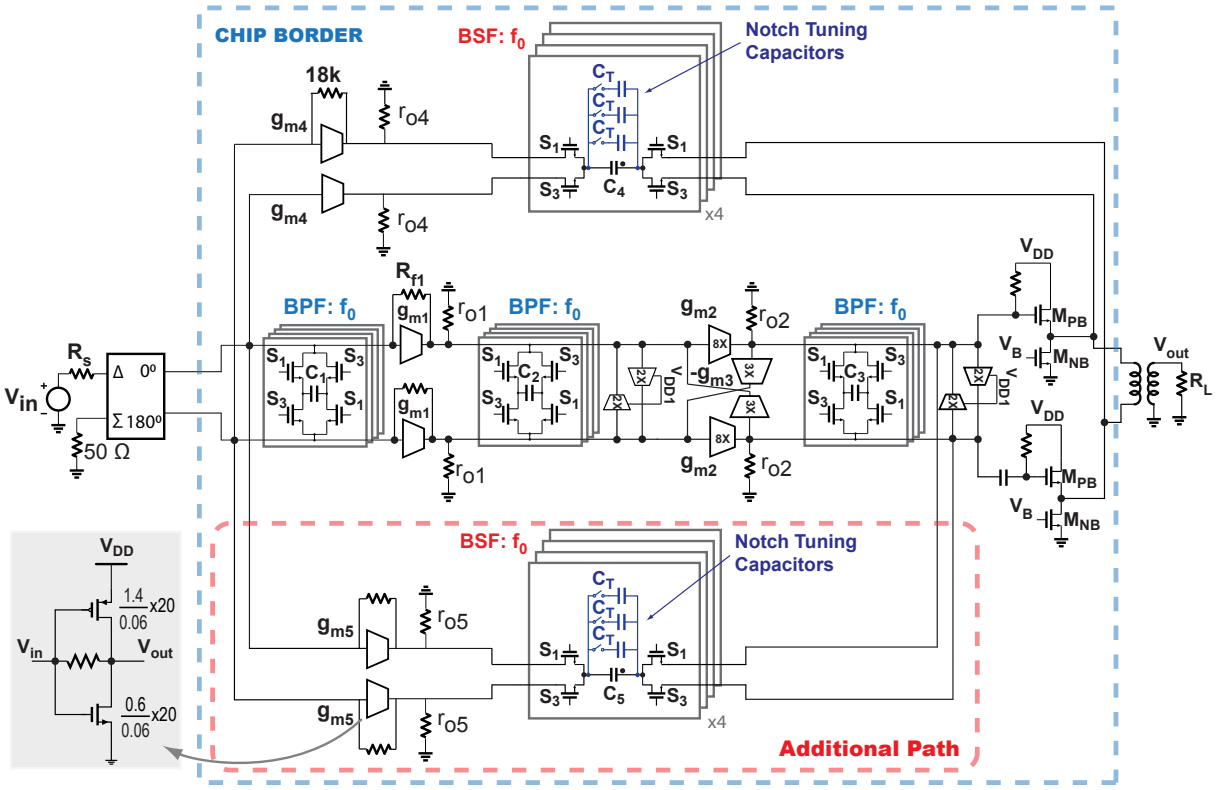

Fig. 18. The schematic of the improved filter design with two TZs. Inset: The g_{m5} cell used in the bottom BS filter.

g_{m3} reduces the BW of the filter. A compromise between gain, NF, area, and power consumption needs to be reached when determining the g_{m1} and g_{m3} values.

Fig. 19 shows a simplified schematic of the filter to calculate the stopband rejection A_{sb} (difference between passband and stopband voltage gain) of the filter. A_{sb} can be found, assuming a perfect duty cycle, as

$$\frac{1}{|A_{sb}|} = \frac{\sqrt{2}g_{m1}}{g_{m3}} \times \text{sinc}^2\left(\frac{\pi}{4}\right) \times \frac{1 + g_{m2}g_{m3}R_{sw}^2}{g_{m1}g_{m2}R_{sw^2} + (g_{m4} - g_{m5})R_{sw}} \times \left(1 + \frac{R_s}{R_{sw}}\right). \quad (26)$$

We would like to reduce R_{sw}, g_{m2} and g_{m3} to increase the stopband rejection. The BW shrinks if either g_{m2} and g_{m3} is reduced. From noise point of view, we would like to increase g_{m2} and reduce g_{m3}.

Shown in Fig. 20, the proposed filter is compared with a 6^{th} order all-pole bandpass filter. The filter has more close-in selectivity (~20 dB better at 40 MHz offset) compared with the all-pole filter due to the creation of close-in TZ. The ultimate out-of-band rejection is worsened due to the cancellation of the BP poles. However, the rejection is still relatively high (40–50 dB) and additional low-Q bandpass filters could be easily integrated to provide further suppression.

Slight tuning of the clock bias voltage also helps to create deeper TZs because it can compensate for the non-ideal duty cycle due to parasitics, layout imperfections, and finite switching time (Fig. 10). However, this does not shift the TZ frequency significantly. The simulated frequency response of the filter with different clock bias voltage is shown in Fig. 17.

A common drawback of N-path filtering is the harmonic folding associated with their time-variant nature [16]. Due to the comb-filter like characteristic, an N-path filter folds back from input frequencies around $(KN \pm 1)f_s$ to the desired band around f_s, where f_s is the switching frequency. The strongest term which result in down-conversion in a 4-path filter is the 3^{rd} harmonic. As a result, increasing the number of paths will increase the distance between f_s and the first folded component around $(N-1)f_s$. However, generating non-overlapping clocks with a high number of phases is difficult at RF as it generally requires very high frequencies (N times the switching frequency). Also, the dynamic power dissipation and parasitic capacitance also increases due to the use of high number of phases.

There are two options to counteract this problem. A low-pass pre-filter can be used in front of the N-path filter to sufficiently suppress harmonic folding, which does not necessarily have to be tunable. In a differential configuration, second harmonic folding is cancelled which relaxes the pre-filter transition band. The alternate option is to use harmonic rejection mixers instead of simple switches that are commonly used in N-path filter. However, each harmonic rejection mixer requires roughly N switches and impedances. This means that the area required for switches and impedances scales with N^2 which may be problematic for large N [47].

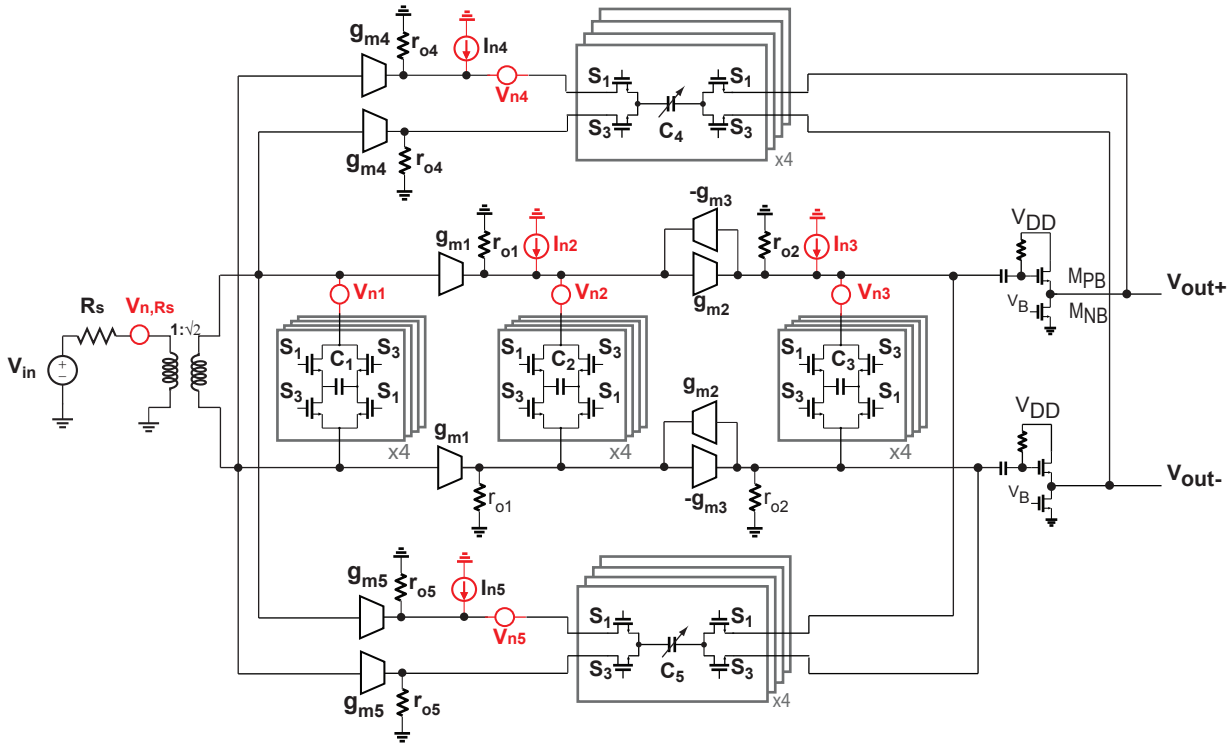

Fig. 22. The equivalent noise sources shown at different places to calculate the overall noise factor of the filter.

C. Noise Analysis

The equivalent noise model for all the sources are shown in Fig. 22, where $V_{n=1,2,3,4,5}$ represent the switch resistance noise of different N-path sections and $I_{n=2,3,4,5}$ represent the noise contribution of the G_m cells and r_{o1}, r_{o2}, r_{o4} and r_{o5} on each node. The low pass counterpart of the filter is used to find the noise transfer function from the noise sources to the baseband voltages and the noise transfer function to the output can be obtained by superposition with a scaling factor of $\mathrm{sinc}^2\left(\frac{\pi}{N}\right)$ [17]. The noise contribution from each of the noise sources are calculated separately and the total output noise is divided by the gain of the filter to find the input-referred noise. As an example, the noise current due to g_{m1} is $4kT\gamma g_{m1}$ and the noise excess factor due to g_{m1} will be approximately $4kT\gamma g_{m1}/4kTR_s(g_{m1}A_1)^2 = \gamma/g_{m1}R_sA_1^2$, where $A_1 = \mathrm{sinc}\left(\frac{\pi}{N}\right)$. The noise contribution of different noise sources to the output node can be found by exploiting the same procedure. Assuming the RF input port is matched to the antenna and $g_{m2}g_{m3}R_{sw}^2 \gg 1$, the noise factor of the receiver is given by

$$F \simeq 1 + \underbrace{\frac{\gamma}{g_{m1}R_sA_1^2}}_{g_{m1}} + \underbrace{\frac{\gamma}{g_{m1}^2R_sg_{m2}r_{o1}^2A_1^2}}_{g_{m2}} + \underbrace{\frac{R_{sw}}{R_s}\times\left(\frac{g_{m3}}{g_{m1}A_1}\right)^2}_{R_{sw}} + \underbrace{\frac{\gamma g_{m3}}{g_{m1}^2A_1^2R_s}}_{g_{m3}} + \underbrace{\frac{\gamma g_{m4}}{R_s}\times\left(\frac{g_{m3}}{g_{m1}g_{MPB}A_1}\right)^2\times\left(\frac{1}{R_{BS1}}\right)^2}_{g_{m4}} + \underbrace{\frac{\gamma g_{m5}r_{o2}^2}{R_s}\left(\frac{g_{m3}}{g_{m1}A_1}\right)^2\times\left(\frac{1}{R_{BS2}}\right)^2}_{g_{m5}} + \underbrace{\frac{g_{m,neg1}}{(g_{m1}A_1)^2R_s}}_{g_{m,neg1}} + \underbrace{\frac{g_{m,neg2}}{(g_{m1}A_1)^2g_{m2}^2r_{o1}^2}}_{g_{m,neg2}} \tag{27}$$

where γ is the noise parameter of the MOSFET and R_{BS1}, R_{BS2} are the insertion loss of the BS filters at the center frequency.

There is an additional contribution to the noise factor due to noise folding. The noise folding mechanism is shown in Fig. 23. The noise sources located at $(1+kN)f_{LO}$ fold back to f_{LO} with a gain of $1/|1+KN|$, where $k = \pm1, \pm2...$ and $k \neq 0$. For $N = 4$, the first folding start from 3^{rd} harmonic and the folding back gain is $1/3$ or -9.54 dB. For each of the noise source, the additional factor due to noise folding is

$$\sum_{n=-\infty, n\neq 0}^{\infty} \left|H_{n,RF}(j\omega)V_{n,N_s}\left[j(\omega - n\omega_s)\right]\right|^2, \tag{28}$$

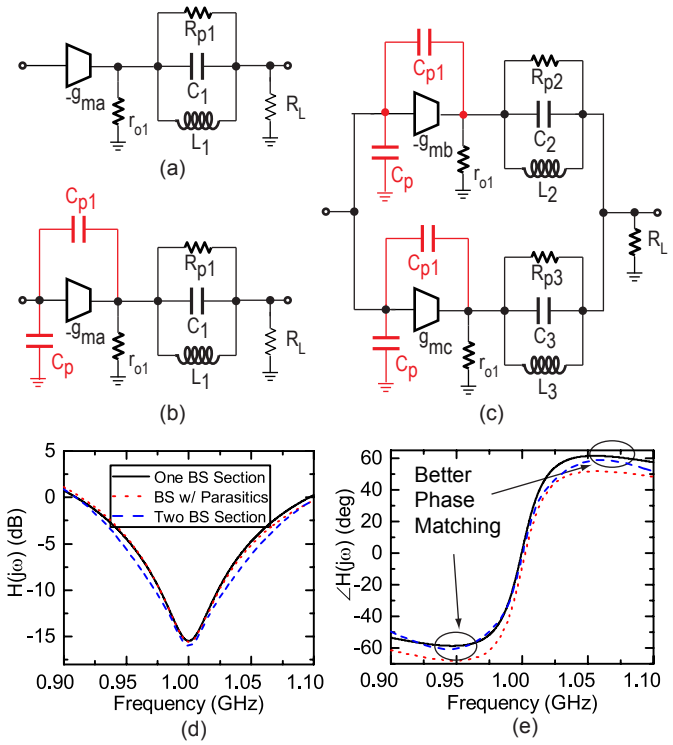

Fig. 16. One BS section with a g_m cell (a) without parasitic capacitance (b) with parasitic capacitance. (c) A second BS section is added to adjust the frequency response. (d) Magnitude and (e) phase response with and without parasitics for one and two BS sections. Adding the second BS path allows one to fine tune the magnitude and phase to create deeper notches.

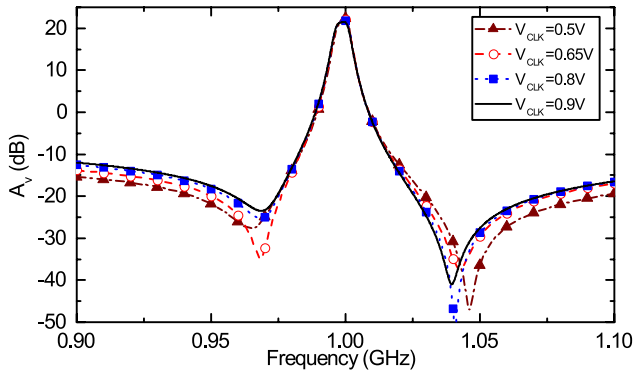

Fig. 17. Simulated filter performance at various clock bias levels.

where n indicates the harmonic number of f_s, $H_{n,RF}(j\omega)$ is the n^{th} harmonic transfer function associated with the frequency nf_s, and N_s represents different noise sources. However, the output noise around the LO harmonics is much smaller compared with the LO first harmonic [13], [48]. The noise contribution from g_{m4} and g_{m5} is negligible at the center frequency due to the use of bandstop filters after those blocks. The noise transfer function of R_{sw} for the bandpass resonators is a notch function and therefore the noise contribution of switches used in the bandpass resonators is relatively suppressed at the center frequency of the filter. On the other hand, the noise transfer function of R_{sw} for the bandstop resonators is a bandpass structure. However, the

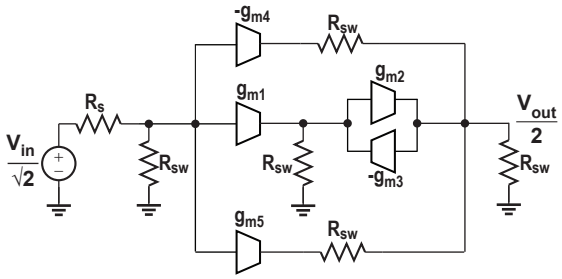

Fig. 19. A simplified schematic of the filter to calculate the stopband rejection. The baseband capacitors are shorted to ground for frequencies far from the passband of the filter and $\sqrt{2}$ is the voltage gain of the balun.

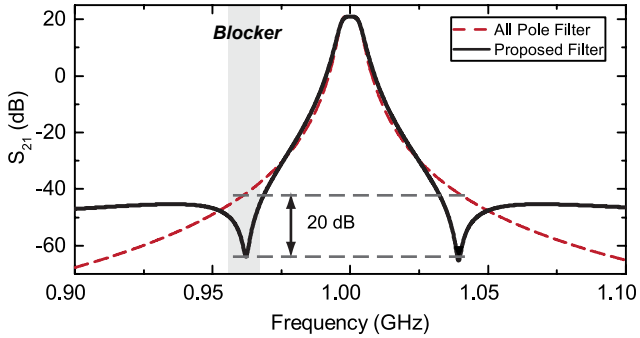

Fig. 20. Simulated comparison between all pole filter and the proposed filter.

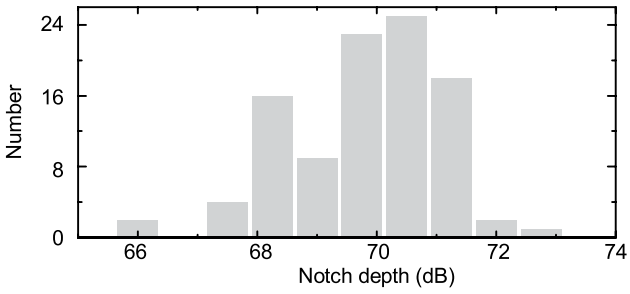

Fig. 21. Monte Carlo simulation of the maximum TZ depth with PVT variations in 100 runs.

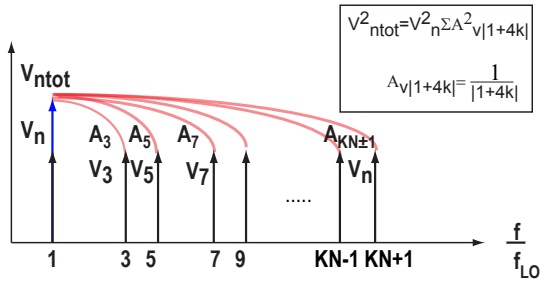

Fig. 23. Folding back of noises located at $|1+4k|f_{LO}$ to f_{LO}.

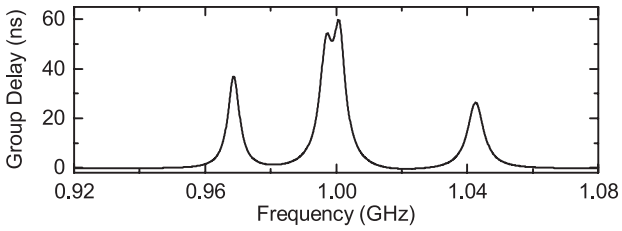

Fig. 24. Simulated group delay of the proposed filter.

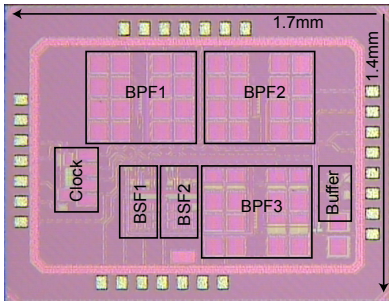

Fig. 25. Chip micrograph of the fabricated filter. Notice that the BS blocks occupy a much smaller area than the BP ones.

effect is negligible due to the use of bandstop filters after those blocks. From (30), we can see that the noise factor is reduced significantly by increasing g_{m1}. However, there is a trade-off between noise, power consumption and the linearity. The linearity degrades and the power consumption increases if we make g_{m1} very large.

VII. Filter Implementation Details

Large NMOS RF switches of $W/L = 80\,\mu m/60\,nm$ (on-resistance of approximately $4.2\,\Omega$) are used to reduce the noise, non-linearity and mismatch between them. The switches are driven by 25% duty cycle 4-phase non-overlapping clocks. Baseband capacitors are made differential in the bandpass section to save area. MIM capacitor with underlying metal are used for the baseband capacitors. The resistors are realized with N+ poly resistor without silicide. Each switch is biased at 900-mV DC voltage (VCLK) to provide full 1.2-V swing to maximize the linearity of the switches. The g_{m5} cell is shown in the inset of Fig. 18. The negative sign in Fig. 14 can be easily obtained by flipping the connection of the top bandstop filter in a differential configuration.

Monte Carlo simulation of TZ depth with PVT variations in 100 runs is shown in Fig. 21. The TZ depth varies from 66 dB to 73 dB at different process corners.

The simulated group delay of the proposed filter is shown in Fig. 24. The addition of the transmission zeros does not significantly affect the group delay variation for in-band signals. However, the group delay variation at the transmission zero frequencies is not very important as the filter provides high attenuation at those frequencies.

VIII. Measurement Results

The filter is fabricated in 65-nm CMOS technology. The chip has an area of 2.4 mm^2 including bonding pads (Fig. 25). The chip is wirebonded and tested on a printed circuit board. An off-chip balun (MACOM MABA-010247-2R1250) is used to transform a single-ended signal to a differential signal. The typical insertion loss of the balun is 1 dB.

A. Frequency Response

Fig. 26(a&b) show the measured S_{21} and S_{11} over the entire tuning range of 0.1–1.4 GHz. The filter shows a gain of 21.5-24 dB, and 3-dB bandwidth of 9.8-10.2 MHz. The parasitic

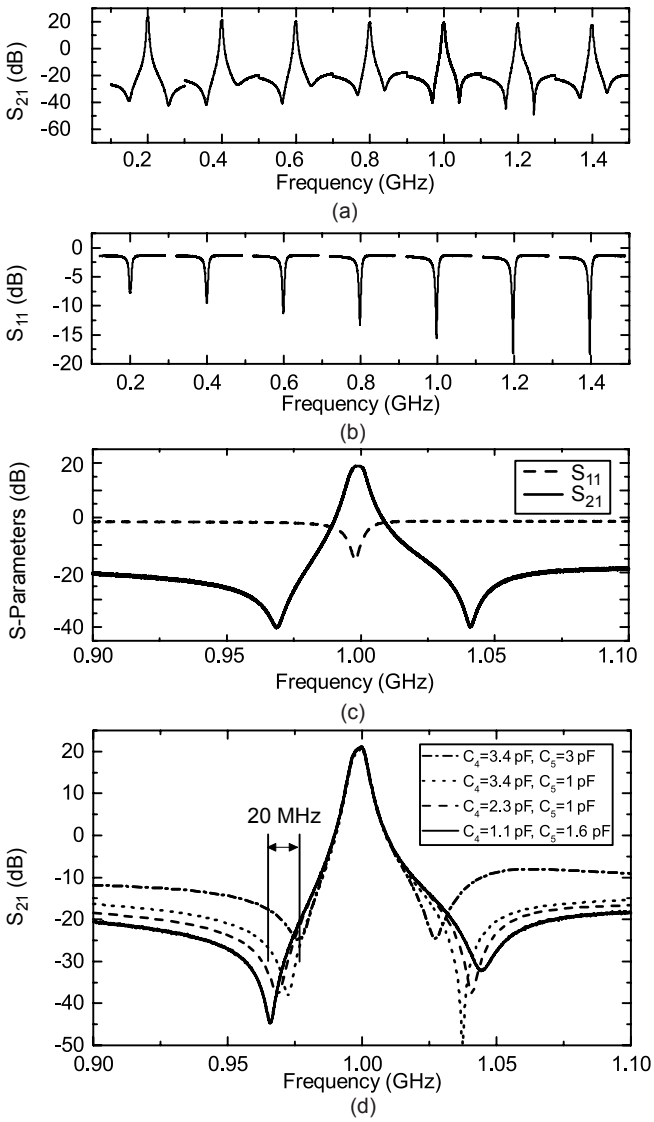

Fig. 26. (a&b) Select measurement result of S_{21} and S_{11} of the fabricated filter over the frequency tuning range. (c) Close-up of the measured S_{21} and S_{11} of the fabricated filter at 1 GHz. (d) Measured TZ tuning performance.

capacitance at each node of the filter modifies the equivalent resistance of that node. As a result, the Q-factor of the filter decreases for higher center frequencies and reduces the gain. The filter draws 27.3 mA, each output buffer draws 4.7 mA and the LO chain draws 3.9 mA to 22.7 mA from 1.2 V in the whole tuning range. The LO feedthrough to the input port of the filter is -58 dBm at a center frequency of 1 GHz.

Fig. 26(c) shows the s-parameters of the filter at 1 GHz. At 1 GHz, the filter has a 23-dB gain with a passband ripple of 0.6 dB and a 3-dB bandwidth of 9.8–10.2 MHz. Transmission zeros are created on both sides of the passband with a minimal offset of 25 MHz and are tunable across 20 MHz range with up to 60 dB rejection. To the best of the authors knowledge, this represents the closest close-in TZ demonstrated in on-chip tunable filters.

The locations of the TZs can be tuned by changing the bank of capacitors (C_T) in the top and bottom BS sections as shown

in Fig. 18. Example measurement results at a center frequency of 1 GHz are shown in Fig. 26(d). The measurement result shows approximately 20 MHz of TZ frequency tuning on both sides of the passband. Tuning of g_{m4} also helps to shift the TZ frequency because it changes the bandstop gain. As the TZs move closer to the passband, the TZ rejection reduces because of a deterioration in the phase matching criteria.

B. Noise Figure

Over the tuning range of 0.1–1.4 GHz, the filter has a measured noise figure (NF) of 3–4.2 dB. The theoretical, simulated and measured NF of the filter over the tuning range is shown in Fig. 27(a). For the theoretical noise calculation, $R_{BS1} = R_{BS2} \approx 30$. The NF is higher at high frequencies as the gain of the filter decreases. The off-chip balun loss is de-embedded in the NF measurement.

Measured NF with various blocker power level is shown in Fig. 27(b) with $f_{LO} = 1$ GHz. In this test, the blocker is placed at the TZ frequency ($\sim$40 MHz offset). The NF increases with increasing blocker power due to reciprocal mixing of the blocker and the LO phase noise. The proposed filter can tolerate an 8-dBm blocker with NF$<$10 dB.

Simulations are carried out to demonstrate the effect of reciprocal mixing. When the blocker mixes with LO phase noise, it deposits additional noise in the receive channel proportional to the blocker amplitude. The simulated phase-noise of on-chip 4-phase LO signals (S_1, S_2, S_3 and S_4) with frequency of 1 GHz from a noisy external signal generator (Keysight E8663D) with frequency of $4f_{lo}$ is shown in Fig. 28(a). The SSB phase noise at various frequency offest (e.g. -143 dBc/Hz at 100 KHz offset) is obtained from the equipment data sheet and specified in Spectre to run the simulation. The simulated NF with noisy and noiseless external clock generator for different blocker power levels are shown in Fig. 28(b). The measured NF is very close to the simulation as shown in Fig. 28(b) and Fig. 27(b).

The measured NF at various blocker frequencies with respect to the center frequency (1 GHz) is shown in Fig. 27(c). The blocker power was set to 0 dBm for this measurement. The measured NF shows a dip at TZ frequency ($\sim$ 40 MHz) due to significant suppression of blocker at that frequency.

C. Linearity

To evaluate the linearity of the filter, two-tone IIP3 and compression measurements were carried out. Results are shown in Fig. 29(a&b). With the filter tuned to 1 GHz, the two tones are placed at 1.002 GHz and 1.003 GHz for the in-band IIP3 measurement, and 1.045 GHz and 1.092 GHz for the out-of-band IIP3 measurement. The out-of-band IIP3 and blocker 1-dB compression point (B1dB) are shown in Fig. 29(a). The B1dB is measured by placing an interfering signal at the TZ frequency and observing the compression behavior of the in-band signal while increasing the power of the interferer. B1dB is around 8 dBm over the tuning range. Out-of-band and in-band IIP3 measured at 1 GHz center frequency are shown in Fig. 29(b).

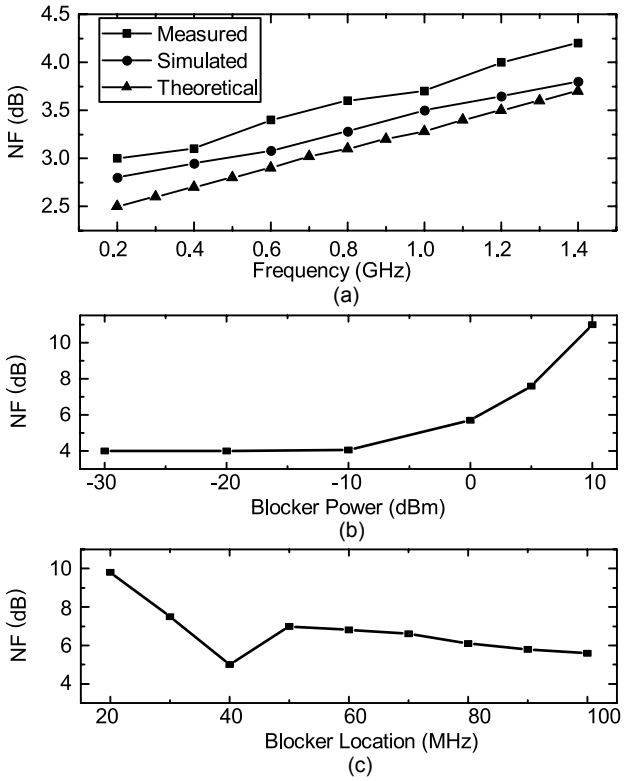

Fig. 27. Measured NF of the filter over (a) the frequency tuning range; (b) the blocker power, (c) the blocker frequency (offset from the carrier frequency).

D. Comparison with other works

The proposed filter is compared with the state-of-the-art receivers and filters in Table. II. The proposed filter shows advantages in creating two adjustable deep transmission zeros on both sides of the passband with low power consumption. A critical advantage is that TZs can be created extremely close (25 MHz) to the passband.

IX. Conclusion

A tunable bandpass filter with two adjustable transmission zeros has been presented in this paper. The TZs are created by the frequency selective cancellation of the transmitted signal from two parallel paths. Due to the tunability of the TZs, the proposed filter can handle strong dynamic blockers in close proximity to the passband and as such show promises as front-end filters for software-defined radio applications.

References

[1] M. N. Hasan, Q. Gu, and X. Liu, "Tunable blocker-tolerant RF front-end filter with dual adaptive notches for reconfigurable receivers," *International Microwave Symposium*, May 2016.

[2] J. Mitola, "Cognitive radio—an integrated agent architecture for software defined radio," Ph.D. dissertation, KTH, The Royal Institute of Technology, 2000.

[3] F. K. Jondral, "Software-defined radio: Basics and evolution to cognitive radio," *EURASIP J. Wirel. Commun. Netw.*, vol. 2005, no. 3, pp. 275–283, Aug. 2005.

[4] A. A. Abidi, "The path to the software-defined radio receiver," *IEEE Journal of Solid-State Circuits*, vol. 42, no. 5, pp. 954–966, May 2007.

[5] R. G. Machado and A. M. Wyglinski, "Software-defined radio: Bridging the analogdigital divide," *Proceedings of the IEEE*, vol. 105, no. 3, pp. 409–423, March 2015.

TABLE II

PERFORMANCE COMPARISON.

	Chen [20]	Luo [22]	Hedayati [26]	Zhou [33]	Darvishi [17]	This work
Circuit Type	Receiver	LNA	Receiver	Receiver	Filter	Filter
CMOS Technology	65 nm (LP)	32 nm (SOI)	65 nm	65 nm	65 nm	65 nm
Frequency (GHz)	0.5–3	0.4–6	0.1–2.8	0.3–1.7	0.1–1.2	0.1–1.4
Max Gain (dB)	38	10	50	19–34	25	23
BW (MHz)	1–30	15	–	2–76	8	10.2
# of Notches	2	2	–	–	–	2
Notch offset (MHz)	20	250	–	–	–	25-45
Notch tunability (MHz)	-	5	–	–	–	20
Notch depth[2](dB)	20	45	–	–	–	55
NF (dB)	3.8–4.7	3.6–4.9	1.8	4.2–5.6	2.8	3–4.2
IIP3 (OOB) (dB)	10	36	5	12–14	26	23
Blocker P1dB	-1 dBm	>17 dBm	–	>2 dBm	7 dBm	8 dBm
LO leakage to RX Input (dBm)	–	-55	-82	-55	-64	-58
Area (w/ pads)	7.8	0.88	0.9[3]	1.2	1.96	2.4
Power (mW)	76–96[4]	81–209	27–40	146.6–155	18–57.3	50–73

[2]From Maximum Gain to Notch depth
[3]Excluding clock buffer power consumption
[4]Active area

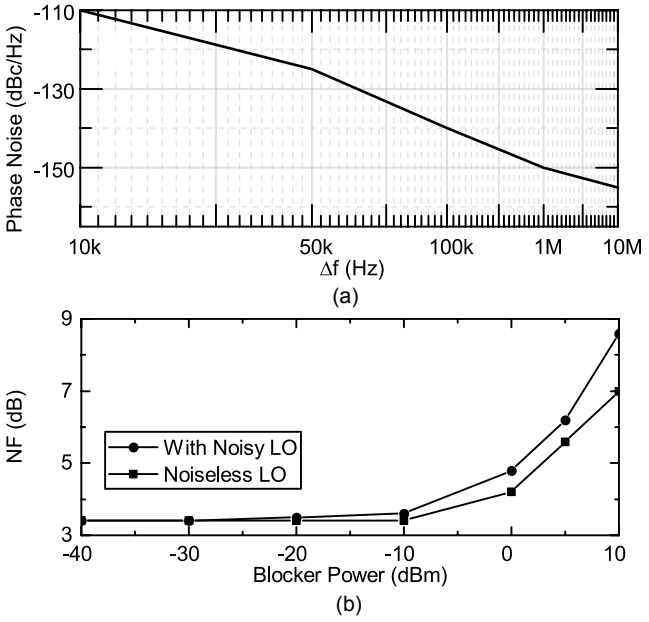

Fig. 28. (a) The simulated phase-noise of on-chip 4-phase LO signals ($f_{LO} = 1\,\text{GHz}$) from a noisy external signal generator (at $4f_{lo}$) (b) NF with noisy and noiseless LO signals. The phase noise of the external signal generator is specified in Spectre.

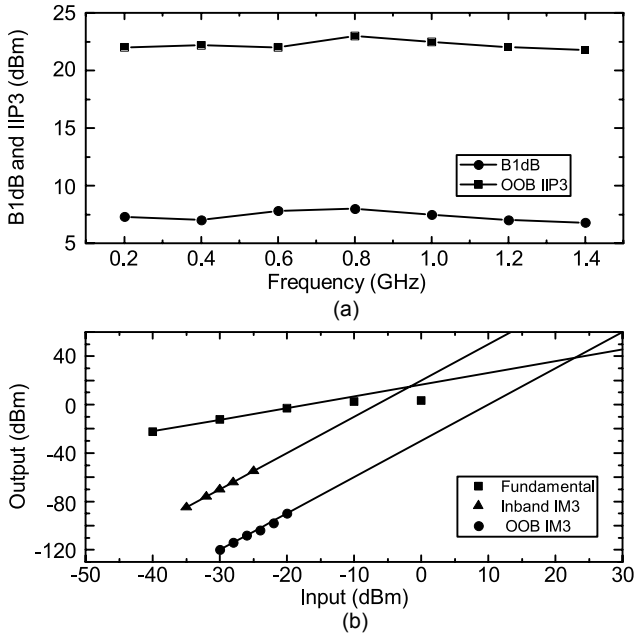

Fig. 29. (a) Measured out-of-band IIP3 and blocker 1-dB compression point over the whole tuning range. (b) Measured out-of-band IIP3 and in-band IIP3 at 1GHz.

[6] "3GPP TS 36.331 v 13.1.0, April 2016; Technical specification group radio access network; evolved universal terrestrial radio access (E-UTRA) and radio resource control (RRC); overall description; release 13."

[7] Z. Ru, N. A. Moseley, E. A. Klumperink, and B. Nauta, "Digitally enhanced software-defined radio receiver robust to out-of-band interference," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 12, pp. 3359–3375, 2009.

[8] A. Mirzaei, H. Darabi, J. C. Leete, X. Chen, K. Juan, and A. Yazdi, "Analysis and optimization of current-driven passive mixers in narrow-band direct-conversion receivers," *Solid-State Circuits, IEEE Journal of*, vol. 44, no. 10, pp. 2678–2688, 2009.

[9] J. Borremans, G. Mandal, V. Giannini, B. Debaillie, M. Ingels, T. Sano, B. Verbruggen, and J. Craninckx, "A 40 nm cmos 0.4–6 ghz receiver resilient to out-of-band blockers," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 7, pp. 1659–1671, 2011.

[10] C.-Y. Yu, I. S.-C. Lu, Y.-H. Chen, L.-C. Cho, C.-H. E. Sun, C.-C. Tang, H.-H. Chang, W.-C. Lee, S.-J. Huang, T.-H. Wu *et al.*, "A saw-less gsm/gprs/edge receiver embedded in 65-nm soc," *Solid-State Circuits, IEEE Journal of*, vol. 46, no. 12, pp. 3047–3060, 2011.

[11] A. Mirzaei, H. Darabi, and D. Murphy, "Architectural evolution of integrated m-phase high-q bandpass filters," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 59, no. 1, pp. 52–65, Jan 2012.

[12] D. Murphy, H. Darabi, A. Abidi, A. A. Hafez, A. Mirzaei, M. Mikhemar, and M.-C. F. Chang, "A blocker-tolerant, noise-cancelling receiver suitable for wideband wireless applications," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 12, pp. 2943–2963, 2012.

[13] C. Andrews and A. C. Molnar, "A passive mixer-first receiver with digitally controlled and widely tunable rf interface," *Solid-State Circuits, IEEE Journal of*, vol. 45, no. 12, pp. 2696–2708, 2010.
[14] ——, "A passive-mixer-first receiver with baseband-controlled rf impedance matching, 6db nf, and 27dbm wideband iip3," in *2010 IEEE International Solid-State Circuits Conference-(ISSCC)*, 2010.
[15] L. E. Franks and I. W. Sandberg, "An alternative approach to the realization of network transfer functions: The n-path filter," *The Bell System Technical Journal*, vol. 39, no. 5, pp. 1321–1350, Sep. 1960.
[16] A. Ghaffari, E. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, 2011.
[17] M. Darvishi, R. van der Zee, and B. Nauta, "Design of active N-path filters," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 12, pp. 2962–2976, Dec 2013.
[18] M. Darvishi, R. van der Zee, E. A. Klumperink, and B. Nauta, "Widely tunable 4th order switched g-c band-pass filter based on n-path filters," *Solid-State Circuits, IEEE Journal of*, vol. 47, no. 12, pp. 3105–3119, 2012.
[19] R. Chen and H. Hashemi, "A 0.5-to-3 GHz software-defined radio receiver using discrete-time RF signal processing," *Solid-State Circuits, IEEE Journal of*, vol. 49, no. 5, pp. 1097–1111, 2014.
[20] ——, "Reconfigurable receiver with radio-frequency current-mode complex signal processing supporting carrier aggregation," *IEEE Journal of Solid-State Circuits*, vol. 50, no. 12, pp. 3032–3046, Dec. 2015.
[21] ——, "Reconfigurable SDR receiver with enhanced front-end frequency selectivity suitable for intra-band and inter-band carrier aggregation," in *Solid- State Circuits Conference - (ISSCC), 2015 IEEE International*, Feb. 2015, pp. 1–3.
[22] C. K. Luo, P. S. Gudem, and J. F. Buckwalter, "A 0.4-6-GHz 17–dBm B1dB 36–dBm IIP3 channel-selecting low-noise amplifier for SAW-less 3g/4g FDD diversity receivers," *IEEE Transactions on Microwave Theory and Techniques*, 2016.
[23] S. Aggarwal and X. Xiao, "Methods and apparatuses for implementing variable bandwidth RF tracking filters for reconfigurable multi-standard radios," Dec 2013, uS Patent 9,136,815.
[24] J.-Y. Bae, S. Kim, H.-S. Cho, I.-Y. Lee, D. Ha, and S.-G. Lee, "A CMOS wideband highly linear low-noise amplifier for digital TV applications," *IEEE Transactions on Microwave Theory and Techniques*, vol. 61, no. 10, pp. 3700–3711, 2013.
[25] S. Ganesan, E. Sánchez-Sinencio, and J. Silva-Martinez, "A highly linear low-noise amplifier," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 54, no. 12, pp. 4079–4085, 2006.
[26] H. Hedayati, W.-F. A. Lau, N. Kim, V. Aparin, and K. Entesari, "A 1.8 db nf blocker-filtering noise-canceling wideband receiver with shared tia in 40 nm cmos," *Solid-State Circuits, IEEE Journal of*, vol. 50, no. 5, pp. 1148–1164, 2015.
[27] S. H. Abdelhalem, P. S. Gudem, and L. E. Larson, "Tunable cmos integrated duplexer with antenna impedance tracking and high isolation in the transmit and receive bands," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 62, no. 9, pp. 2092–2104, 2014.
[28] M. Elkholy, M. Mikhemar, H. Darabi, and K. Entesari, "Low-loss integrated passive cmos electrical balance duplexers with single-ended lna," *IEEE Transactions on Microwave Theory and Techniques*, vol. 64, no. 5, pp. 1544–1559, 2016.
[29] R. J. Cameron, R. Mansour, and C. M. Kudsia, *Microwave Filters for Communication Systems : Fundamentals, Design and Applications*. Wiley, 2007.
[30] S. Ayazian and R. Gharpurey, "Feedforward interference cancellation in radio receiver front-ends," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 902–906, 2007.
[31] A. Goel, B. Analui, and H. Hashemi, "Tunable duplexer with passive feed-forward cancellation to improve the rx-tx isolation," *Circuits and Systems I: Regular Papers, IEEE Transactions on*, vol. 62, no. 2, pp. 536–544, 2015.
[32] T. O'Sullivan, R. A. York, B. Noren, and P. M. Asbeck, "Adaptive duplexer implemented using single-path and multipath feedforward techniques with bst phase shifters," *Microwave Theory and Techniques, IEEE Transactions on*, vol. 53, no. 1, pp. 106–114, 2005.
[33] J. Zhou, P. Kinget, and H. Krishnaswamy, "A blocker-resilient wideband receiver with low-noise active two-point cancellation of >0dBm TX leakage and TX noise in RX band for FDD/Co-existence," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, 2014, pp. 352–353.
[34] S. Darfeuille, J. Lintignat, R. Gomez-Garcia, Z. Sassi, B. Barelaud, L. Billonnet, B. Jarry, H. Marie, and P. Gamand, "Silicon-integrated differential bandpass filters based on recursive and channelized principles and methodology to compute their exact noise figure," *IEEE Transactions on Microwave Theory and Techniques*, vol. 54, no. 12, pp. 4381–4396, Dec. 2006.
[35] M. N. Hasan, Q. Gu, and X. Liu, "Reconfigurable blocker-tolerant RF front-end filter with tunable notch for active cancellation of transmitter leakage in FDD receivers," *International Symposium on Circuits and Systems (ISCAS)*, May 2016.
[36] C. Luo, P. Gudem, and J. Buckwalter, "A 0.2–3.6-GHz 10-dBm B1dB 29-dBm iip3 Tunable filter for transmit leakage suppression in SAW-less 3G/4G FDD receivers," *IEEE Transactions on Microwave Theory and Techniques*, 2015, early Access.
[37] S. Aggarwal and M. N. Hasan, "Tunable RF N-path filter," Aug. 2016, US Patent 9,407,482.
[38] J. B. Thomas, "Cross-coupling in coaxial cavity filters–A tutorial overview," *IEEE Transactions on Microwave Theory and Techniques*, 2003.
[39] R. Gomez-Garcia and J. I. Alonso, "Design of sharp-rejection and low-loss wide-band planar filters using signal-interference techniques," *IEEE microwave and wireless components letters*, vol. 15, no. 8, pp. 530–532, Aug. 2005.
[40] P. W. Wong and I. C. Hunter, "A new class of low-loss high-linearity electronically reconfigurable microwave filter," *IEEE Transactions on Microwave Theory and Techniques*, vol. 56, no. 8, pp. 1945–1953, Aug. 2008.
[41] J. M. Muoz-Ferreras and R. Gomez-Garcia, "A digital interpretation of frequency-periodic signal-interference microwave passive filters," *IEEE Transactions on Microwave Theory and Techniques*, vol. 62, no. 11, pp. 2633–2640, Nov 2014.
[42] M. N. Hasan, S. Aggarwal, Q. Gu, and X. Liu, "Tunable N-path RF front-end filter with an adaptive integrated notch for FDD/co-existence," in *Circuits and Systems (MWSCAS), 2015 IEEE 58th International Midwest Symposium on*, 2015, pp. 1–4.
[43] D. Psychogiou, R. Gómez-García, R. Loeches-Sánchez, and D. Peroulis, "Hybrid acoustic-wave-lumped-element resonators (awlrs) for high- bandpass filters with quasi-elliptic frequency response," *IEEE Transactions on Microwave Theory and Techniques*, vol. 63, no. 7, pp. 2233–2244, Jul. 2015.
[44] A. Ghaffari, E. Klumperink, and B. Nauta, "Tunable N-path notch filters for blocker suppression: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 48, no. 6, pp. 1370–1382, 2013.
[45] B. Razavi, *RF Microelectronics*, 2nd ed. Upper Saddle River, NJ, USA: Prentice Hall Press, 2011.
[46] M. N. Hasan and S. Aggarwal, "Tunable RF channel select filter," Sep 2015, US Patent 9,130,532.
[47] L. C. Fortgens, "Approximation of an ideal bandpass filter using an n-path filter with overlapping clocks and harmonic rejection," Master's thesis, University of Twente, 2012.
[48] Z. Lin, P. I. Mak, and R. P. Martins, "Analysis and modeling of a gain-boosted N-path switched-capacitor bandpass filter," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 61, no. 9, pp. 2560–2568, Sept 2014.

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