Tunable Blocker-Tolerant RF Front-end Filter with Dual Adaptive Notches for Reconfigurable Receivers

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***Abstract*—This paper presents a novel design of a highly tunable active bandpass filter with adjustable notches close to the passband. The filter is based on two-path signal cancellation and consists of a tunable bandpass filter in parallel with a tunable bandstop filter. This combination ensures the correct amplitude and phase relationship across a wide tuning range to create adjustable transmission notches without sacrificing the gain of the passband. The proposed filter is implemented with high-Q N-path filter/resonator blocks in a 65-nm CMOS process. The passband of the filter is tunable from 0.2 GHz to 1.2 GHz with a 3-dB bandwidth of 5.8–6.2 dB, a gain of 18.5–21 dB, a noise figure of 4.5–6.2 dB, and a total power consumption of 33–70 mW. Transmission notches are created on both sides of the passband with a minimal offset of 20 MHz and are tunable across a 20 MHz range with up to 46 dB rejection. The blocker 1-dB compression point is 8 dBm and the out-of-band IIP3 is 18 dBm. The reported filter provides a promising solution to multi-standard, multi-frequency software-defined radio applications.**

***Index Terms*—Bandpass filter, blocker rejection, CMOS, N-path, notch filter, Switched-capacitor, tunable.**

I. Introduction

Modern CMOS receivers utilize high-Q surface acoustic wave (SAW) filters to attenuate large out-of-band blockers, which may desensitize the receiver. Multiple SAW filters are necessary to cover different frequency standards, which increases the cost and form factor. To reduce the cost and size of the transceiver chips, multiple dedicated narrowband radios can be replaced with one widely tunable radio covering the frequency bands. However, a wideband receiver has no selectivity and must withstand strong blockers as well as the desired signal. Maintaining a high dynamic range is challenging in presence of large blockers, which might be located very close or even between the desired frequency channels. To fulfil these requirements, a tunable bandpass filter is necessary which can attenuate blockers at the corresponding frequencies.

Various on-chip techniques to handle out-of-band blockers have been proposed recently. A low noise amplifier is presented in [1] which creates dual notches on both sides of the passband to suppress TX leakage. The gain of the amplifier is low and the notch is also not tunable. In [2], a tunable bandpass filter is proposed with two concurrent notches on both sides of the passband. The linearity is constrained due to the use of a front stage RF low noise transconductance amplifier (LNTA). A feed-forward interference cancellation technique is proposed in [3] to attenuate large interferers. Two high pass filters are used in parallel with a LNA to create nearby notches. However, the lack of any input filtering imposes relatively challenging linearity requirement on the LNA input devices, thus compromising the NF. A low power filter with single sided tunable notch to handle TX leakage is presented in [4].

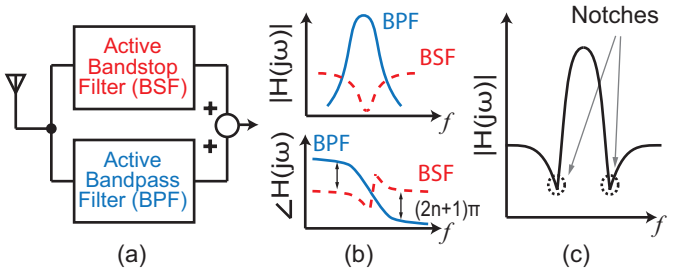

Fig. 1. (a) A parallel combination of Bandpass and Bandstop filter creates two notch outside the passband of the filter (b) Magnitude and phase response of individual bandpass and bandstop filters (c) Notch creation where the magnitude of both paths are same and phase difference is $(2n+1)\pi$.

In this paper, a tunable bandpass filter with two adaptive tunable notches is proposed. The primary concept of the filter is depicted in Fig. 1, which uses a tunable bandpass filter and a tunable bandstop filter in parallel. The gain and phase of the two paths can be controlled to ensure out-of-phase cancellation of the transmitted signal, therefore creating two transmission notches close to the passband. The use of a tunable bandstop filter ensures that the correct phase relationship (Fig. 1) is maintained over a wide tuning range and that minimal perturbation to the passband gain of the active bandpass filter is introduced.

II. Reconfigurable Bandpass Filter

The proposed filter design starts with a prototype of a 3-pole bandpass filter (BPF) and a 1-pole bandstop filter (BSF) connected in parallel as shown in Fig. 2(a) to create two notches outside the passband. The BPF consists of three shunt resonators connected with two admittance inverters. The shunt bandpass resonators can be implemented with shunt configuration of N-path filters [5] and the series bandstop resonators can be implemented with series configuration of N-path filters as shown in Fig. 2(b). The detailed schematic of the proposed filter is shown in Fig. 2(c). The admittance inverters are implemented with active gyrators implemented each with two back-to-back transconductance (g_m) cells. Active gyrators are used to ensure the impedance transformation characteristics over a wide tuning range. To lower the power consumption and to increase the dynamic range of the filter, the first gyrator is

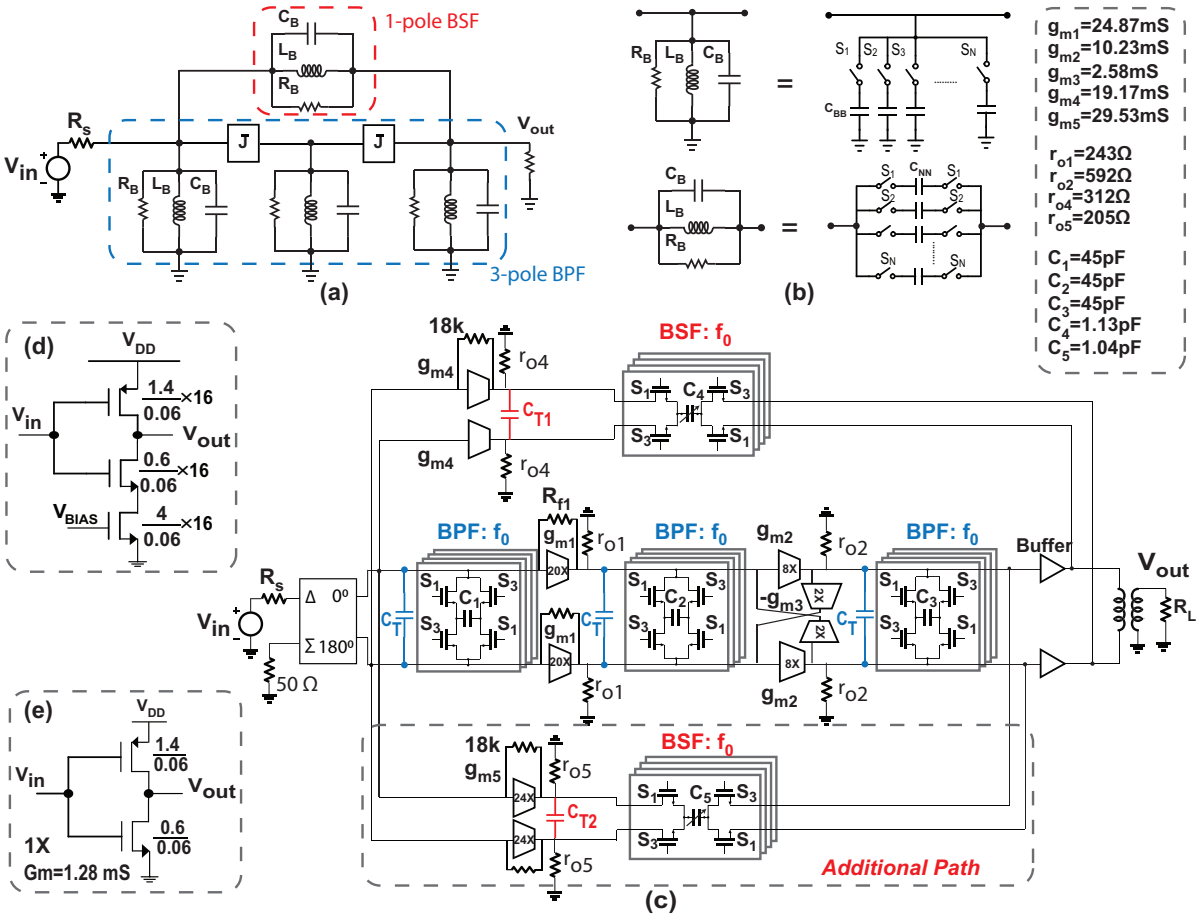

Fig. 2. (a) Parallel and series LC tanks can be emulated with their N-path counterparts (b) Lumped model of the proposed filter (c) Detailed schematic diagram of the proposed filter (d) The g_{m4} cell (e) The unit g_m cell that is used in the filter with different scaling factors (g_{m1}, g_{m2}, g_{m3} and g_{m5}).

substituted by a single G_m cell, g_{m1}. This effectively reduces the BPF prototype to a cascade of a 1-pole filter with a 2-pole filter. The overall roll-off of the BPF still follows a 3-pole characteristic due to the impedance isolation by g_{m1}. A differential configuration is exploited for the filter design.

A. Parasitic Capacitance

One major nonideality that limits the operation of the switched-capacitor block at high frequencies is the parasitic capacitance. The parasitic capacitance contains contributions from the switches and the signal routing lines. The parasitic capacitance is labeled as C_T in the bandpass sections and C_{T1} in the bandstop section. The parasitic capacitance creates asymmetry in the amplitude and phase response and as a result, only one notch can be created. To generate two notches, an additional bandstop path is added in the filter as shown in Fig. 2(b). To reduce the mutual interaction between the top and bottom bandstop sections, the top bandstop section is connected at the output of the buffer.

B. Implementation of the Filter Building Blocks

All the g_m cells (g_{m1}, g_{m2}, g_{m3} and g_{m5}), except g_{m4} are based on a self-biased inverter unit cell (Fig. 2(e)). The g_m values, output impedance r_o, and the baseband capacitors C_{BB} are listed in Fig. 2. The current in g_{m4} is controlled through V_{BIAS} for better matching of the two paths. NMOS switches of W/L=80 μm/60 nm are driven by 25% duty cycle 4-phase non-overlapping clocks. A master clock at 4 times the switching frequency is applied from off-chip and a flip-flop based divider divides the input clock by four. To reduce even-order harmonics, a differential clocking scheme is utilized. Baseband capacitors are made differential in the bandpass section to save area. MIM capacitor with underlying metal are used for the baseband capacitors. The resistors are realized with N+ poly resistor without silicide. The switches are realized with NMOS RF transistors. Large switches are used to reduce the noise, non-linearity and mismatch between them. Each switch is biased at 950-mV DC voltage to provide full 1.2-V swing to maximize the linearity of the switches. The input impedance of the filter at the resonant frequency f_s can be found by

$$Z_{in} \simeq R_{sw} + \gamma \frac{R_{f1}}{1 + g_{m1}(r_{o1} || Z_{sh})} || Z_{sh} \qquad (1)$$

where $\gamma = \frac{2}{\pi^2}$ and $Z_{sh} = \frac{4\gamma}{1-4\gamma}(R_s + R_{sw})$. The values of R_{f1} and g_{m1} are chosen properly for input impedance matching.

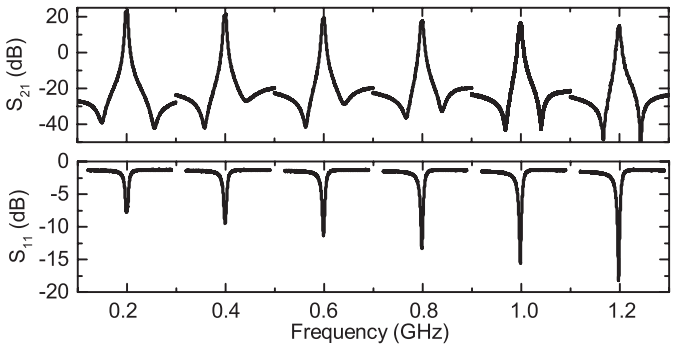

Fig. 3. Measured S_{21} and S_{11} at different frequencies.

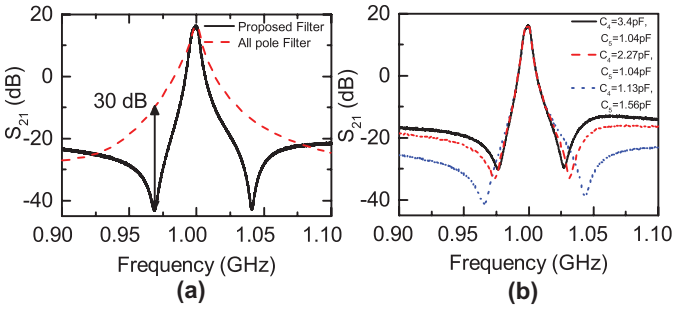

Fig. 4. (a) The filter is compared with an all-pole filter. (b) Notch tuning is shown at a few representative frequencies.

III. Measurement Results

The filter is realized in 65-nm CMOS technology. The measured S_{21} and S_{11} over the whole tuning range are shown in Fig. 3(a). The filter has 21 dB gain provided by the $g_{\rm m}$ cells as shown in Fig. 3(a) with passband ripple of 0.6 dB and 3-dB bandwidth of 6.2 MHz. The parasitic capacitance at each node of the filter modifies the equivalent resistance of that node. As a result, the Q-factor of the filter increases as the clock frequency reduces and the gain increases.

In Fig. 4(a), the proposed filter is compared with a 3-pole all-pole bandpass filter. The filter has more close-in selectivity ($\sim$30 dB better) compared with the all-pole filter due to the creation of notches, which is necessary for carrier aggregation. However, the ultimate out-of-band rejection is slightly worse due to the cancellation of the poles.

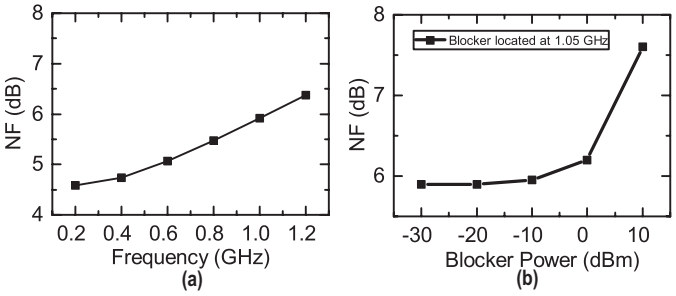

Fig. 5. (a) Measured NF of the proposed filter over the tuning range. (b) Measured NF with different blocker power at 1 GHz.

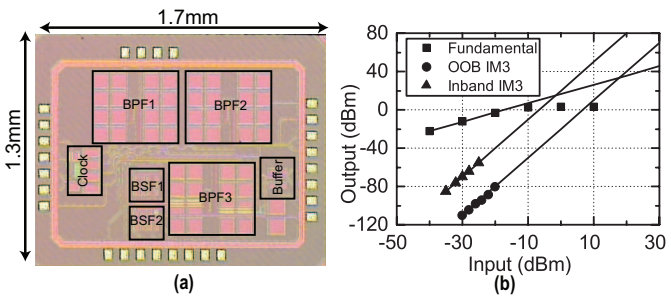

Fig. 6. (a) Chip micrograph of the proposed filter. (b)Measured IIP3.

The notch frequency tuning by changing the bandstop capacitances at a few representative frequencies are shown in Fig. 4(b). A switched bank of MOS capacitors are used to shift the notch frequency. The measurement result shows approximately 20 MHz of notch tuning on both sides of the passband. Tuning of g_{m4} also helps to shift the notch frequency as the bandstop gain can be changed. The noise figure (NF) of the filter over the tuning range is shown in Fig. 5(a) and the NF with various blocker power level is shown in Fig. 5(b) with $f_{LO} = 1$ GHz. In this test, the blocker was located at the notch frequency ($\sim$50 MHz offset). Two-tone IIP3 measurement results are shown in Fig. 6(b). The two tones are located at 1.002 GHz/1.003 GHz for the in-band IIP3 measurement, and 1.045 GHz/1.092 GHz for the out-of-band IIP3 measurement. The proposed filter is compared with the state-of-the-art receivers and filters in Table. I. The proposed filter shows advantages in creating two adjustable notches on both sides of the passband with low power consumption.

TABLE I
Performance Comparison.

	Luo [1]	Chen [2]	Zhou [6]	This work
Circuit Type	LNA	Receiver	Receiver	Filter
CMOS Tech	32 nm (SOI)	65 nm (LP)	65 nm	65 nm
Frequency (GHz)	0.4–6	0.5–3	0.3–1.7	0.2–1.2
Max Gain (dB)	10	38	19–34	21
BW (MHz)	15	1 –30	2–76	6.2
# of Notches	2	2	–	2
NF (dB)	3.6–4.9	4.8	4.2–5.6	4.5–6.2
NF (dB) w/ 0-dBm blocker @ offset	- -	5.7 -	- -	6.5 50 MHz
Blocker P1dB	>17 dBm	-1 dBm	>2 dBm	8 dBm
IIP3 (OOB) (dB)	36	10	12–14	18
Area (w/ pads)	0.88	7.82	1.2	2.2
Power (mW)	81–209	96–150	146.6–155	33–70

IV. Conclusion

A novel tunable bandpass filter with two adjustable notches has been presented in this paper. The notches are created by the frequency selective cancellation of the transmitted signal from two parallel paths. Due to the tunability of the notches, the proposed filter can handle strong dynamic blockers very close to the passband and as such show promises as front-end filters for software-defined radio applications.

REFERENCES

[1] C. kai Luo, P. Gudem, and J. Buckwalter, "0.4–6 GHz,17-dBm B1dB, 36-dBm IIP3 channel-selecting, low-noise amplifier for SAW-less 3G/4G FDD receivers," in *Radio Frequency Integrated Circuits Symposium (RFIC), 2015 IEEE*, 2015, pp. 299–302.

[2] R. Chen and H. Hashemi, "Reconfigurable SDR receiver with enhanced front-end frequency selectivity suitable for intra-band and inter-band carrier aggregation," in *IEEE International Solid- State Circuits Conference (ISSCC), 2015*, 2015, pp. 1–3.

[3] S. Ayazian and R. Gharpurey, "Feedforward interference cancellation in radio receiver front-ends," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 54, no. 10, pp. 902–906, 2007.

[4] M. Hasan, S. Aggarwal, Q. Gu, and X. Liu, "Tunable N-path RF front-end filter with an adaptive integrated notch for FDD/co-existence," in *Circuits and Systems (MWSCAS), 2015 IEEE 58th International Midwest Symposium on*, 2015, pp. 1–4.

[5] A. Ghaffari, E. Klumperink, M. C. M. Soer, and B. Nauta, "Tunable high-Q N-path band-pass filters: Modeling and verification," *IEEE Journal of Solid-State Circuits*, vol. 46, no. 5, pp. 998–1010, 2011.

[6] J. Zhou, P. Kinget, and H. Krishnaswamy, "A blocker-resilient wideband receiver with low-noise active two-point cancellation of >0dBm TX leakage and TX noise in RX band for FDD/Co-existence," in *IEEE International Solid-State Circuits Conference (ISSCC) Digest of Technical Papers*, 2014, pp. 352–353.