Ortho-Mode Sub-THz Interconnect Channel for Planar Chip-to-chip Communications

Bo Yu, Yu Ye, Xuan Ding, Yuhao Liu, Zhiwei Xu, Xiaoguang "Leo" Liu, and Qun Jane Gu

***Abstract*—This paper presents for the first time the design, fabrication, and demonstration of a dielectric waveguide based ortho-mode sub-THz interconnect channel for planar chip-to-chip communications. By combining the proposed new transition of microstrip line to dielectric waveguide orthogonally, the ortho-mode transition is constructed to form an ortho-mode channel. The measured minimum insertion losses for the E_{y11} mode and the E_{x11} mode are 6.6 dB with 20.3 GHz 3-dB bandwidth and 6.5 dB with 55.2 GHz 3-dB bandwidth, respectively. The simulation and measurement results agree well with each other.**

***Index Terms*—Channel, chip-to-chip, communication, dielectric waveguide, interconnect, micromachined, microstrip line, ortho-mode transition, space division multiplexing, sub-THz, THz.**

I. Introduction

FOR chip-to-chip interconnect, there are two most important factors, energy efficiency, defined as the DC power divided by the data rate, and bandwidth density, defined as the data rate divided by the channel area. On the one hand, the power consumption and cooling cost keep increasing with higher data rate. To mitigate this issue, high energy-efficiency interconnects are required. On the other hand, the CPU pin number increases slowly comparing with the CPU bus bandwidth per wire. To satisfy the requirement of the total bus bandwidth, high bandwidth-density interconnects are highly demanded.

One key factor determining energy efficiency is the channel loss. The transmission line has relatively large loss at high frequencies [1], [2]. The metallic waveguide (MWG) also has higher loss than the dielectric waveguide (DWG) at high frequencies [3]–[8], which can be as high as 0.15 dB/mm for MWGs at 600 GHz [4]. Meanwhile, the attenuation of silicon (Si) is reported as 0.017-0.034 dB/mm at 300-1000 GHz [6], [8]. Therefore, Si DWG is a good candidate for the high energy-efficiency sub-THz/THz interconnect.

High permittivity of Si supports small channel dimensions, which thus results in high bandwidth density. Besides, the space division multiplexing (SDM) technique can further boost the bandwidth density by sharing multiple logical channels through the same physical dielectric waveguide link. Thus, the total bandwidth density with N logical channels is given by

$$\rho_{BW} = \frac{BW \times N}{A_{CHNL}}, \tag{1}$$

where the BW is the channel bandwidth for each mode, the N is the number of the propagated modes, and A_{CHNL} is the effective channel area. The SDM can also combine with the frequency division multiplexing (FDM), the time division multiplexing (TDM) and/or the code division multiplexing (CDM) to further boost the data rate and bandwidth density as illustrated in Fig. 1.

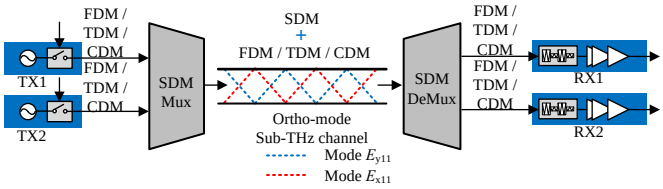

Fig. 1. Proposed DWG based ortho-mode interconnect architecture.

There are two major research areas, optical interconnect and electrical interconnect, to address the interconnect issue. Optical interconnects [9]–[12] have the advantages of low loss and wide bandwidth while the integration of high-efficiency light sources with current CMOS processes is still very challenging. Electrical interconnects [3], [13]–[26] have the merits of compatibility and scalability with silicon processes while with the drawback of high loss at high frequencies. Therefore, both schemes have their own limitations to completely address the interconnect issue.

The Si DWG based sub-THz interconnect, using the spectrum sandwiched between optical and microwave frequencies, had been proposed to solve the interconnect issue by leveraging the advantages of both optical and electrical interconnect approaches: low-loss quasi-optical channels as well as advanced high-speed semiconductor devices [27]–[30]. With this sub-THz channel, the high energy-efficiency and high bandwidth-density single-mode sub-THz interconnect had been demonstrated in [31].

To further boost the bandwidth density, the ortho-mode channel has been studied in this work. The ortho-mode transition or transducer (OMT), known as a polarization duplexer, is a device combining or separating orthogonally polarized signals. The ideal OMT can be modeled as a four-port device

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B. Yu, Y. Ye, X. Ding, Y. Liu, X. Liu, and Q. J. Gu are with the Department of Electrical and Computer Engineering, University of California, Davis, CA 95616 USA (e-mail: boyu@ucdavis.edu; yuye@ucdavis.edu; xxding@ucdavis.edu; yuhliu@ucdavis.edu; lxgliu@ucdavis.edu; jgu@ucdavis.edu)

Z. Xu is with Zhejiang University, China (e-mail: xuzhw@zju.edu.cn)

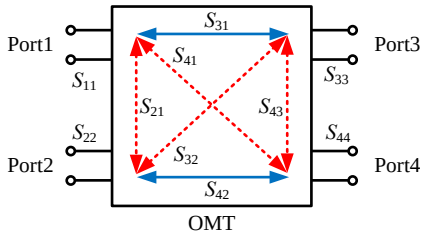

Fig. 2. Four-port OMT model.

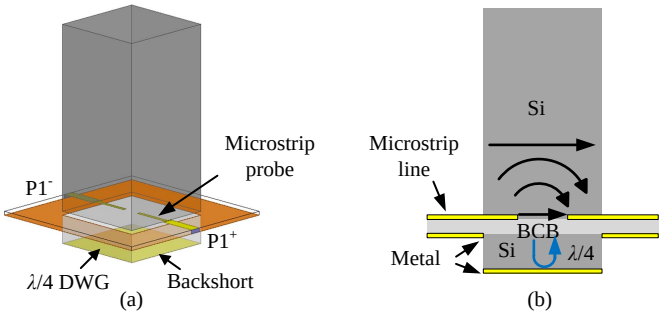

Fig. 3. Differential MSL-to-DWG single-mode transition: (a) Perspective view, and (b) Side view.

as shown in Fig. 2. The 4 × 4 scattering matrix S is given by

$$S = \begin{bmatrix} 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \\ 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \end{bmatrix}. \quad (2)$$

For an ortho-mode channel, the majority research focuses on the MWG based OMT channel, which requires expensive machining and are not compatible with planar structures [32]–[34].

In this work, we have demonstrated a Si DWG based OMT channel with a small channel area and compatible with planar micro-machine processes. The OMT channel consists of a square waveguide and two OMTs. Compared with the authors previous work [35], this paper presents a discussion about a thorough analysis of a single-mode and ortho-mode transitions design, including the difference between single-ended and differential transition feeding, the planar integration considerations, including a bending structure and a backside trench. Besides, the loss distribution for the completed structure is analyzed. With the optimization of two important design parameters, the channel performances are also significantly boosted comparing with [35]. First, the length of the microstrip line is reduced. Second, the metal thickness is increased from 100 nm to 300 nm. Therefore, the channel performance is significantly improved from 8-9 dB to 6.6 dB.

This paper is organized as follows. Section II reviews and presents the design method of the OMT channel and planar integration considerations. Section III discusses the fabrication, measurement, and non-ideality of the OMT sub-THz interconnect channel, which is followed by the conclusion in Section IV.

II. OMT Channel Design

Before discussing the transition design, a DWG design is reviewed. The design of DWG includes several aspects, mode, loss, bandwidth, isolation, etc. For a rectangular DWG, the fundamental mode is E_{y11} or E_{x11}.

The loss of a DWG is determined by several factors, including the dielectric loss of the material, the geometry of the waveguide, and possibilities of mode conversion. Material loss is one of the most critical loss source. [27] has investigated that high resistivity silicon is a good candidate for the DWG. Besides, the bending and discontinuity structures could cause the reflection loss and radiation loss. Also, the additional loss could be from the mode conversion, which is indicated by the effective index of the first several modes [27].

The bandwidth of a DWG is primarily determined by the dispersion characteristics of the chosen mode of the propagating wave and the orthogonality and/or isolation from other modes. For a 500 µm × 500 µm Si DWG with the fundamental mode, the simulated cut-off frequency, which is 3 dB lower than the minimum insertion loss, is 94.7 GHz.

Channel isolation is another key factor for high bandwidth-density and high energy-efficiency communication systems. Higher channel isolation leads to smaller channel space for higher bandwidth density and higher energy efficiency due to smaller coupling noise.

A. Transition Design

The conventional microstrip line (MSL)-to-MWG transition can confine EM waves inside thanks to the metal wall but it is hard to be integrated in planar processes. To solve this issue, the MSL-to-DWG transition could be used. Since the DWG does not have the metal wall, the reference ground is located in infinite for the single-ended MSL-to-DWG transition, which causes large loss. Therefore, a differential probes based MSL-to-DWG transition is proposed to form a differential mode intrinsically to match E_{y11} or E_{x11} mode in the DWG. Fig. 3(a) and (b) show the configuration of the proposed differential MSL-to-DWG single-mode transition. It consists of a DWG, two MSLs, a pair of microstrip probes for the transition, and a backshort on the bottom of the DWG. Since the center operation frequency is set at 175 GHz, the length of each side of the DWG is about 500 µm [27]. With a substrate of 20-µm Bisbenzocyclobutene (BCB) (ε_r = 2.65), the line width of the 50-Ω MSL is 56 µm. With the center opening window between MSLs, the EM waves propagate in both directions, up and down, along the DWG. The backshort is placed λ/4 away from the feeding position to provide out-of-phase signal cancellation and only allow the EM waves propagate along the up direction of the DWG. The differential microstrip probes are used to form the differential mode.

Fig. 4(a) and (b) plot the vectors of the E-field distributions of the transition for the E_{y11} and E_{x11} modes, respectively, which is based on full-wave simulation in ANSYS high frequency structure simulator (HFSS). The EM waves are gradually transitioned from the quasi-TEM in the MSL as shown in Fig. 4(c), to the hybrid mode in the transition as shown in Fig. 4(d), and then to the E_{y11} or E_{x11} mode in the DWG as shown in Fig. 4(e).

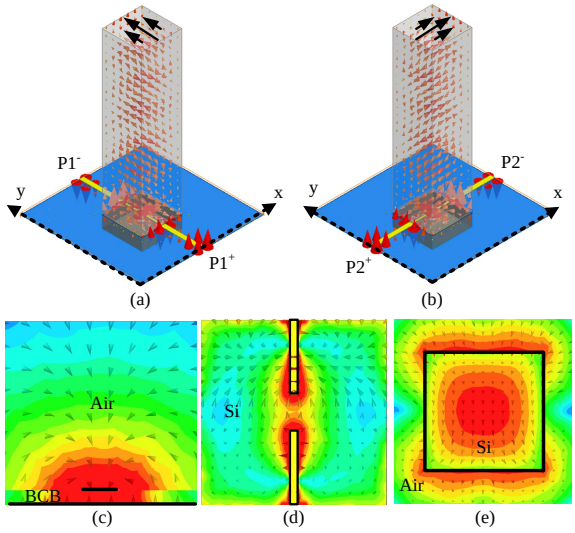

Fig. 4. Simulated vector of the E-field distribution of the transition: (a) E_{y11}, and (b) E_{x11}. Cross section view of the E-field distribution: (c) MSL, (d) Transition interface, and (e) DWG.

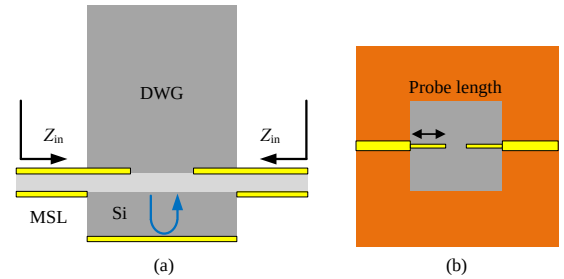

Fig. 5. Schematic of the input impedance Z_{in}: (a) Side view, and (b) Top view.

The essential mechanism of the transition design is the impedance matching. The input impedance of the transition Z_{in}, illustrated in Fig. 5, is determined by the probe length. Fig. 6(a) plots the input impedance versus the probe length and Fig. 6(b) plots the input impedance versus the frequency. To match with 50 Ω, the probe length is 180-200 μm at the frequencies of around 175 GHz. Simulated S_{11} versus the backshort-to-probe distance at 175 GHz is plotted in Fig. 6(c). At the design frequency, $\lambda/4$ in silicon is approximated as 140 μm.

With the differential MSL-to-DWG single-mode transition, an OMT is proposed in this work as shown in Fig. 7. It consists of two single-mode transitions which are placed orthogonally. The magnitude of the E-field distributions for the in-phase mode and quadrature-phase mode combinations are shown in Fig. 8(a) and (b), respectively.

A back-to-back structure is plotted in Fig. 9(a). The two pairs of the differential ports P1$^+$, P1$^-$ and P3$^+$, P3$^-$ are for E_{y11} mode, and that of ports P2$^+$, P2$^-$ and P4$^+$, P4$^-$ are for E_{x11} mode. As shown in Fig. 9(b), the minimum insertion loss is about 2.6 dB with 47.7 GHz 3-dB bandwidth referred to the minimum insertion loss for both modes. The S_{11} is better than -10 dB at the range of 140-200 GHz. The S_{21} is better than -30 dB in the range of 145-187 GHz, and the S_{41} is better than -30 dB in the range of 140-200 GHz.

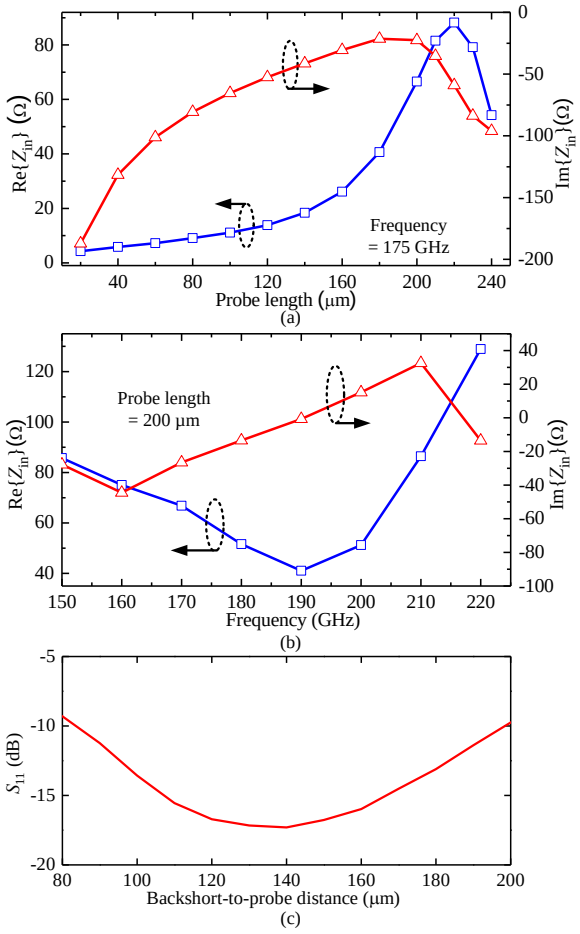

Fig. 6. (a) Simulated input impedance versus the probe length when the frequency = 175 GHz; (b) Input impedance versus the frequency when the probe length = 200 μm; (c) Simulated S_{11} versus the backshort-to-probe distance with the frequency = 175 GHz and probe length = 200 μm.

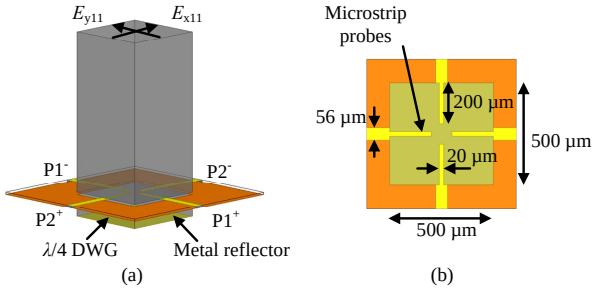

Fig. 7. Structure of the proposed OMT: (a) Perspective view, and (b) Top view.

B. Planar Integration

To convert the differential signals to single-ended signal, the rectangular planar rat-race balun [36], [37] is utilized as shown in Fig. 10(a). With the characteristic impedance of 70 Ω, the line width of the balun is 34 μm. The ratio of the two individual branch lengths is 1:3 to form a 180° phase difference at the center frequency. The lengths of two branches are 295 μm and 975 μm through the optimization.

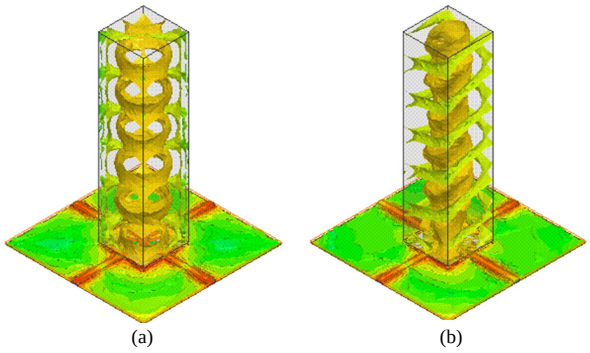

Fig. 8. Simulated magnitude of the E-field distribution with two combination modes: (a) In phase, and (b) Quadrature phase.

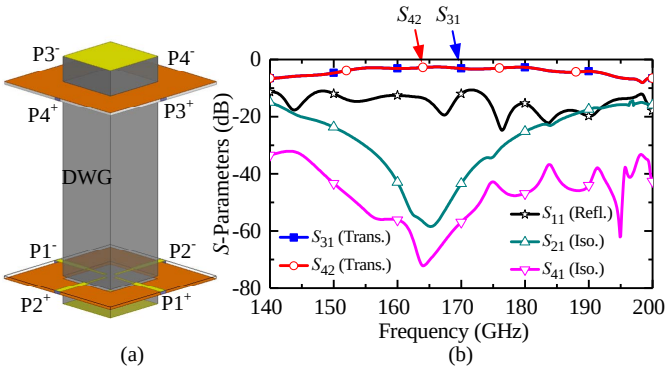

Fig. 9. (a) Back-to-back OMT channel. (b) Simulated S-parameters.

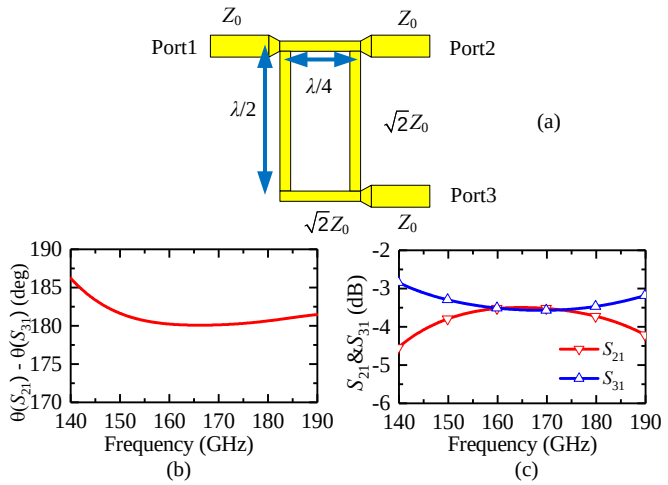

Fig. 10. (a) Schematic of the rectangular planar rat-race balun. (b) Simulated phase difference between S_{21} and S_{31}. (c) Simulated magnitudes of S_{21} and S_{31}.

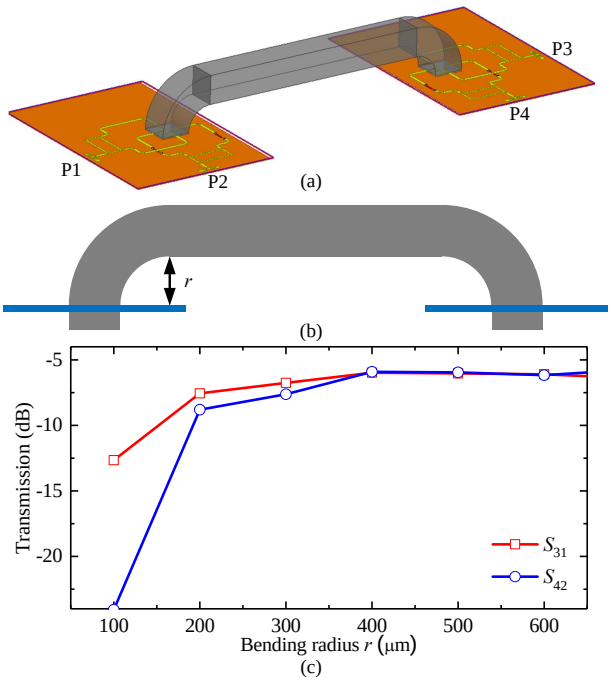

Fig. 11. (a) Perspective view of the planar structure of the OMT channel. (b) Side view of the channel. (c) Simulated transmission loss versus the bending radius r.

The simulated phase difference is less than 7° at the range of 140-190 GHz as shown in Fig. 10(b). The simulated minimum insertion loss for each branch is 3.5 dB as shown in Fig. 10(c). The simulated minimum insertion loss of back-to-back baluns is about 1.0 dB.

To implement the planar chip-to-chip structure, a bended DWG is the most intuitive method as shown in Fig. 11(a) and (b). The DWG bend is a bridge between the straight DWG and planar OMT. The bending radius r is the inner radius of the bend. The cost of a DWG bend is the introduced bending loss for both modes [27]. The bending loss includes two parts, radiation loss and mode conversion loss [27]. For small r compared with the cross section area, both radiation loss and mode conversion loss are severe. As shown in Fig. 11(c), the larger r, the smaller the bending loss is. The insertion loss for each 500 μm × 500 μm bend is about 0.3 dB. Also, the bending losses for two modes are different due to the bending direction. To overcome this issue, a large r is preferred. On the other hand, to enhance the reliability of the structure and reduce the profile of the structure, a small r is preferred. By trading off these considerations, r is set as 400 μm.

The side view of the transition is shown in Fig. 12(a), which consists of a DWG bend, a $\lambda/4$ DWG, and a signal feeding structure. However, the size of the feeding structure is much larger than the $\lambda/4$ DWG so that the transition has reliability issue. To solve the mechanical reliability issue, the substrate of the $\lambda/4$ DWG with a whole piece instead of a single stub is used as shown in Fig. 12(b). However, a whole piece of substrate will introduce the EM wave leakage issue due to the enlarged size of the $\lambda/4$ DWG as shown in Fig. 13(a).

The backside trench is designed to overcome the leakage

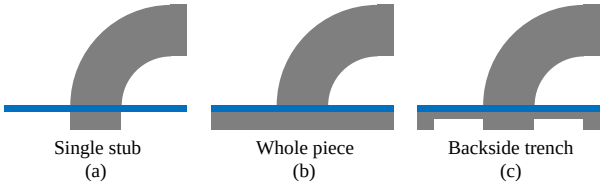

Fig. 12. Side view of the transition with (a) Single stub as substrate, (b) Whole piece as the substrate, or (c) Whole piece with the backside trench.

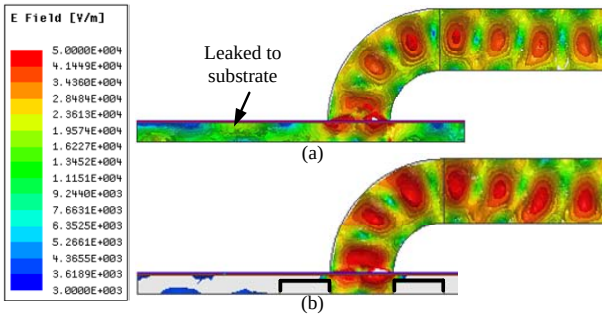

Fig. 13. Magnitude of the E-field distributions: (a) Without backside trench, and (b) With backside trench.

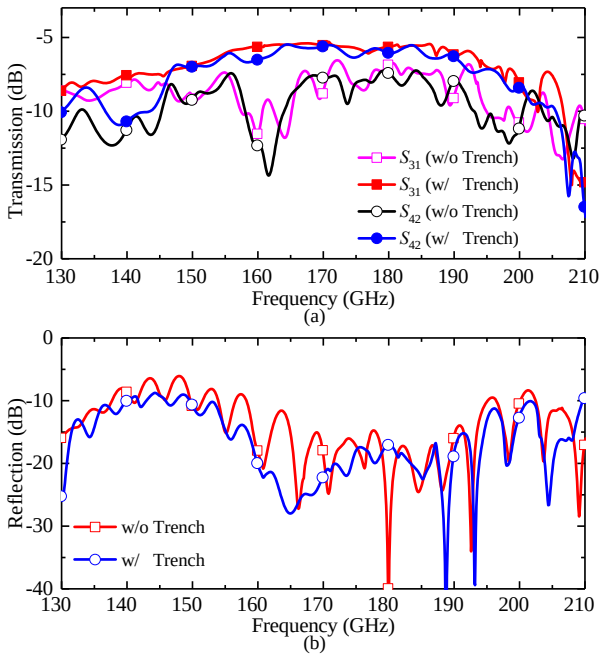

Fig. 14. S-parameter comparisons between without and with backside trench: (a) Transmission, and (b) Reflection.

issue as shown in Fig. 12(c). With the trench, the leakage is significantly reduced as shown in Fig. 13(b). Both performance of the transmission and reflection are improved as shown in Fig. 14. In terms of the electrical performance, a large trench is required; in terms of the mechanical reliability, a small trench size is preferred. The leakage loss will be minimized if the depth and the width of the trench are larger than 60 μm and 400 μm respectively, as shown in Fig. 15.

The completed OMT channel for planar chip-to-chip communications is illustrated in Fig. 16. It consists of a straight DWG, two DWG bends, two transitions, MSLs, four baluns, four GSG-to-MSL transitions, two backshorts, and two backside trenches. To simplify the demonstration, the joined substrate is used instead of two separated substrates. Besides, the overpass trace and vias are utilized to allow a cross-over line. To maintain the symmetry of the differential inputs, a dummy overpass trace and two vias are employed in the path without crossing over as shown in Fig. 16(b). The width and length of the overpass trace are 28 μm and 200 μm, respectively. The size of the vias is 40 μm × 40 μm with a 10-μm depth.

To assemble the DWG onto the OMT, the BCB bonding technique is used. The transmission loss versus the BCB thickness is plotted in Fig. 17. In this design, the bonding thickness is < 2 μm, which is determined by the bonding pressure.

C. Loss Analysis

The simulated results of the completed OMT channel are plotted in Fig. 18. The minimum insertion losses are 5.4 dB and the average insertion losses are 6.4 dB for both modes with larger than 52 GHz 3-dB bandwidth. The S_{21} and S_{41} are better than -20 dB from 140-210 GHz.

To analyze the loss, a completed single-mode structure is drawn in Fig. 19, and the channel is partitioned into several

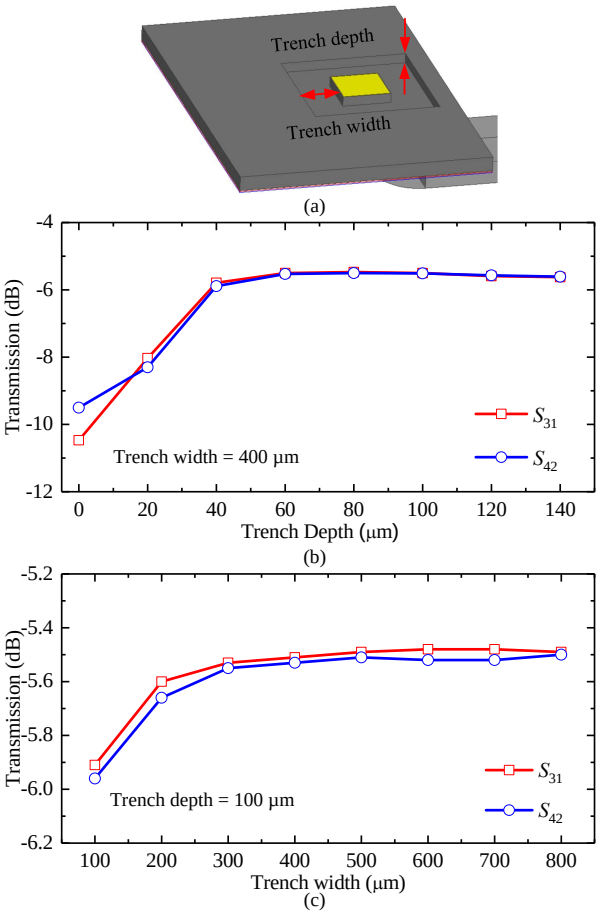

Fig. 15. (a) Bottom view of the OMT. (b) Simulated transmission loss versus the trench depth when the trench width = 400 μm. (c) Simulated transmission loss versus the trench width when the trench depth = 100 μm.

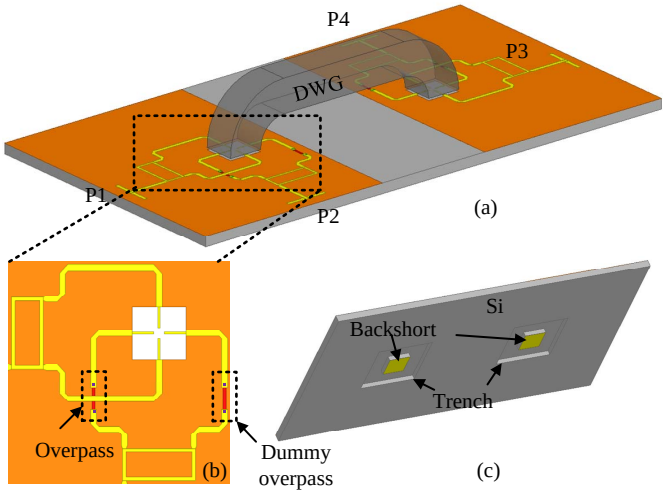

Fig. 16. (a) Perspective view of the top side of the planar OMT channel, (b) Zoomed-in OMT, and (c) Perspective view of the back side of the OMT channel.

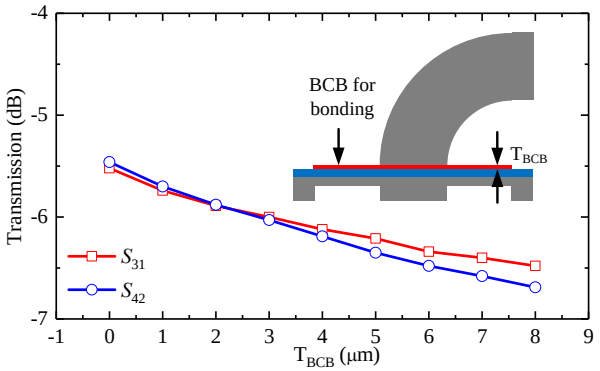

Fig. 17. Simulated transmission loss versus the BCB thickness. The inset shows the side view of the BCB bonding.

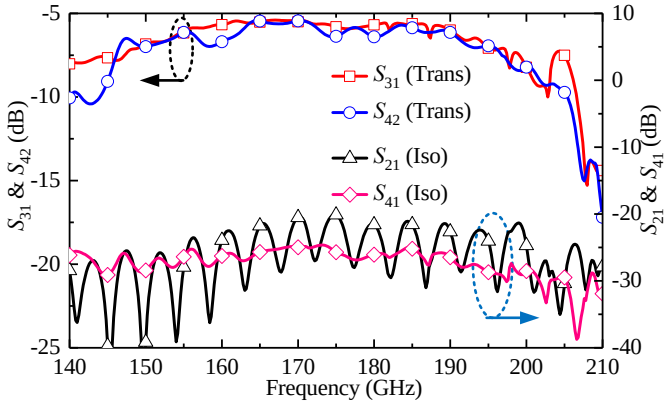

Fig. 18. Simulated S-parameters for the completed planar OMT channel.

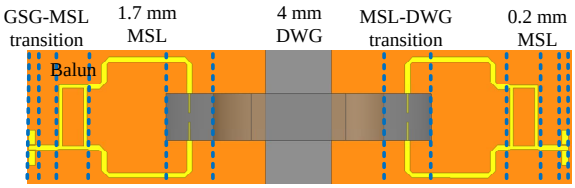

Fig. 19. Top view of the single-mode channel.

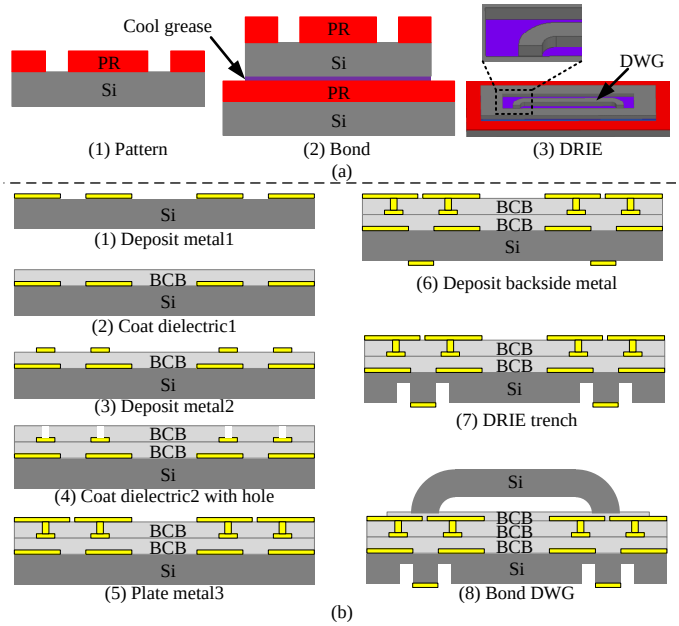

Fig. 20. OMT channel fabrication processes: (a) DWG, and (b) OMT and bonding.

stages. It includes two GSG-to-MSL transitions, two baluns, two 1.7-mm MSLs, two MSL-to-DWG transitions, two DWG bends, and a 4-mm DWG, which cause the losses of 0.2 dB, 1.0 dB, 2.0 dB, 2.44 dB, 0.6 dB, and 0.16 dB, respectively. Because the high resistivity silicon DWG is low-loss, The 4-mm DWG instead of a 10-mm DWG is used to reduce the simulation time and complexity. The core components, the DWG, two bends, and MSL-to-DWG transitions, consume 3.2 dB in total.

III. Experimental Demonstration

A. Fabrication

The OMT channel fabrication includes three steps: the deep etching of the DWG, the construction of the OMT, and the DWG-to-OMT bonding. The DWG fabrication process is summarized in Fig. 20(a). First, a photoresist AZ9260 is used to form a thick feature layer (about 17 μm). Then, a high resistivity (HR) silicon wafer (<100>, $\rho > 1000$ Ω·cm, ε_r = 11.9, and tanδ = 0.001) is adhered on a silicon handle wafer by cool grease. After that, the HR silicon wafer is etched through by deep reactive ion etching (DRIE) process to generate the DWG with bends. Finally, the DWG is picked up and two bending ends are face down.

The OMT fabrication process is summarized in Fig. 20(b). The 150-μm HR silicon is used as handling wafer and the

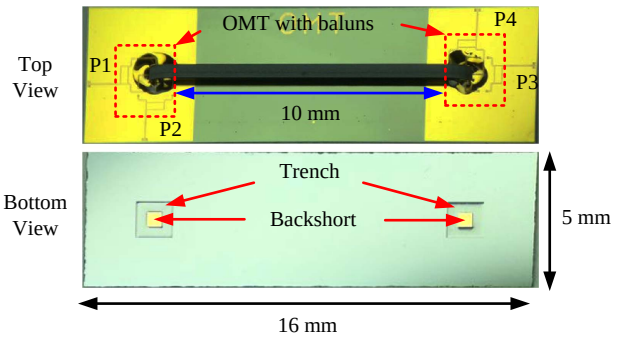

Fig. 21. Photos of the top view and bottom view of the OMT channel.

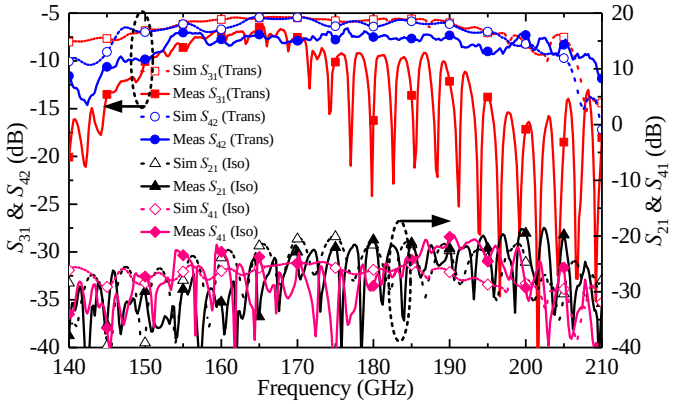

Fig. 22. Comparisons of the simulated and measured S-parameters for the OMT channel.

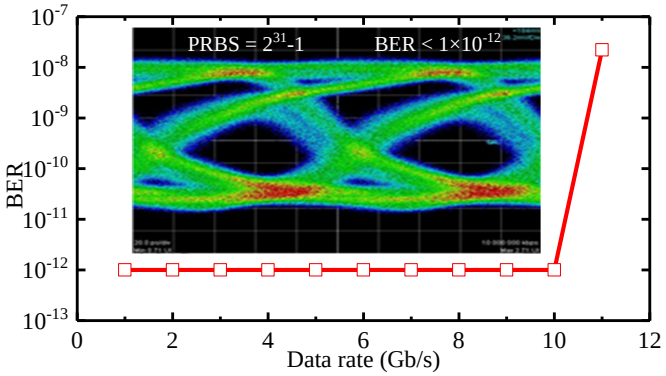

Fig. 23. Measured eye diagram for mode of S_{42} at PRBS $2^{31}-1$ and BER $< 1 \times 10^{-12}$.

BCB 4026-57 (ε_r = 2.65, and tanδ = 0.015 [38]) is used for a thin-film substrate. The coupling structure includes three metal layers and two dielectric layers. Metal1 (50 nm/300 nm Ti/Au) is deposited on the top of the Si wafer. After that, Metal2 is sandwiched between two 10-μm BCB followed by the electrical-plating for Metal3 (2-μm Au). After Metal3 metallization, the wafer is flipped for the backshorts. Finally, the trenches around the backshort are etched by the DRIE process.

With the prepared DWG and OMT, a pick-and-place tool (Finetech Fineplacer PICO A4) is used to bond the DWG to the OMT by an extra BCB layer. The device photos are shown in Fig. 21. The total OMT channel size is 16 mm × 5 mm with a 10-mm straight DWG. Using the center opening window between MSLs in the OMT, the alignment accuracy is achieved less than ± 5 μm.

B. Measurement

The measurement setup consists of an Agilent network analyzer (PNA-X N5247A), a pair of Virginia Diodes frequency converter modules (VDI WR5.1-VNAX), WR-5 (140-220 GHz) S-bend waveguides, and a pair of WR-5 probes. The SOLT (Short, Open, Load, Thru) calibration method is employed to set the reference plane at the probe tip. Limited by our test equipment, only two ports are connected each time while the other two ports are floated thanks to the good isolation between the orthogonal paths.

Fig. 22 plots the comparisons of simulated and measured S-parameters for the OMT channel. The measured minimum insertion losses for the mode E_{y11} and the mode E_{x11} are 6.6 dB with 20.3 GHz 3-dB bandwidth from 151.1 to 171.4 GHz and 6.5 dB with 55.2 GHz 3-dB bandwidth from 150.8 to 206 GHz, respectively. The S_{21} and S_{41} are better than -20 dB in the range of 140-210 GHz.

The measured bit-error rates (BER) versus data rate for the mode of S_{42} is plotted in Fig. 23, together with the eye diagram in the inset. The $2^{31}-1$ PRBS pattern is generated from Anritsu MP2011B. The data rate is up to 10 Gb/s. Due to the limited frequency response, the eye diagram cannot be measured for the mode of S_{31}.

To evaluate the performance of sub-THz interconnect channel, we define a figure of merit (FoM) as

$$FoM = \frac{\rho_{\mathrm{BW}}}{Loss\,|_{\,\mathrm{Unit\,Length}}} = \frac{BW/A_{\mathrm{CHNL}}}{Loss/l_{\mathrm{CHNL}}}, \qquad (3)$$

where BW is the channel bandwidth, ρ_{BW} is the channel bandwidth density, A_{CHNL} is the effective channel area, $Loss$ is the channel loss, and l_{CHNL} is the channel length. Higher operating frequency leads to the increasing of FoM as discussed in [27].

Table I summarizes the proposed channel performance and makes comparisons with the state-of-the-arts. Baseband based interconnect channel [21] has very high bandwidth density due to the small effective channel area, but it is not scalable to higher frequencies. The proposed work have the bandwidth density of 33.3 GHz/mm^2 and the FoM of 832 GHz/mm/dB for the mode E_{y11}, and the bandwidth density of 90.5 GHz/mm^2 and the FoM of 2262 GHz/mm/dB for the modes E_{x11}. For the whole channel, the bandwidth density is 123.8 GHz/mm^2 and the FoM is 3094 GHz/mm/dB with the total bandwidth of 75.5 GHz since these two modes are independent. Compared with the other interconnect channels, our proposed work has higher bandwidth density and achieves the best FoM thanks to the low-loss wide-bandwidth channel and the small effective channel area. [3] has a good FoM but the channel loss is relative high and the integration for planar technologies is relatively complicated.

To analyze the discrepancy between simulation and measurement, the surface roughness, assembly accuracy and non-ideal shape for the DWG have been investigated. Since the

TABLE I
COMPARISON AMONG DIFFERENT HIGH-SPEED INTERCONNECT CHANNEL

Reference	[3]	[19]	[21]	[24]	[25]	[31]	This work
Channel Media	Si Filled MWG	DWG	Stripline	Air	MWG	Single Mode DWG	Orthomode DWG
Center Frequency (GHz)	105	275	dc	135	92.5	165	175
BW (GHz)	49	50	>20	30	35	59	20.3 / 55.2
Channel Length (mm)	N/A	4.8	2.5/3.5	100	300	46.2	10
Channel Loss (dB/mm)	0.12	0.05	2.8	N/A	N/A	0.04	0.04
Channel Cross Setion Area (mm^2)	0.27	0.1	0.01	>1.4*	>3.23*	0.15	0.25
Effective Channel Area (mm^2)	0.27	N/A	0.01	>1.4*	>3.23*	0.61**	0.61**
BW Density (GHz/mm^2)	181.5	N/A	>2000	<21.4	<10.8	96.7	123.8****
FoM (GHz/mm/dB)***	1512	N/A	>714	N/A	N/A	2418	3094****
Planar Integration	Complicated	Easy	Easy	Easy	Hard	Easy	Easy
Scalable to High Frequency	Yes	Yes	No	Yes	Yes	Yes	Yes

* Metallic waveguide horn antenna or metallic waveguide is used. The cross section area is larger than waveguide inner size.
** (Channel Pitch in Width $|_{\mathrm{ISO=30dB}}$) × (Channel Pitch in Height $|_{\mathrm{ISO=30dB}}$).
*** FoM = (BW / Effective Channel Area) / (Channel Loss / Channel Length). **** Total bandwidth is used for the calculation.

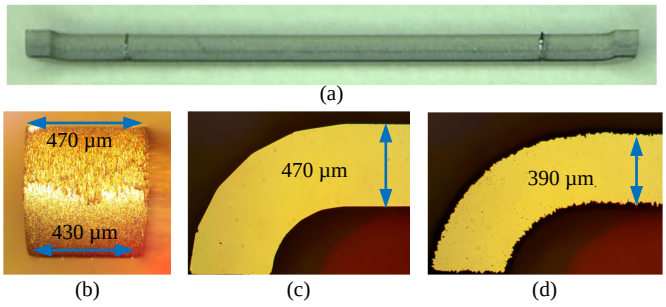

Fig. 24. Photos of the DWG: (a) Bottom view, (b) View of the left transition interface, (c) Front view, and (d) Back view.

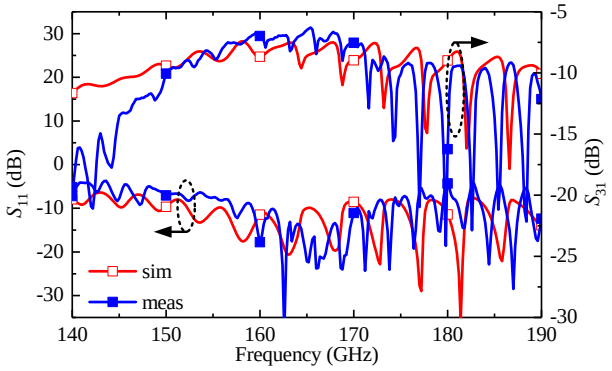

Fig. 25. Comparisons of the simulated and measured S-parameters for E_{y11} mode of the OMT channel with the updated shape.

signal waves are majorly confined inside the DWG, the surface roughness and assembly accuracy have negligible effects on the performance. The most possible factor is the non-ideal fabrication of the DWG with bends as shown in Fig. 24. The shape of the cross section of the DWG becomes polygon instead of square. The front width of the DWG is about 470 μm. The back width is 390-430 μm. To simplify the modeling, a trapezoid shape is used instead of the polygon shape. With the updated shape, the simulated S_{31} matches better with the measured result as shown in Fig. 25. The difference between simulation and measurement in Fig. 25 could be caused by the inaccurate modeling.

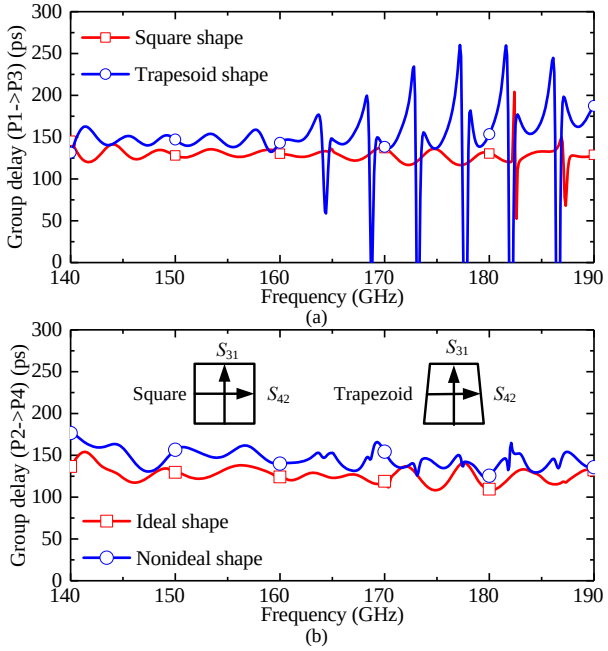

Fig. 26. Simulated group delays for the channel with a square or trapezoid DWG: (a) P1→P3, (b) P2→P4. The insets show the ortho-mode excitations for both square and trapezoid shapes.

The polygon shape for the DWG could be caused by the over-etching. To guarantee all exposed areas are etched through, the etching time is set as about 120% comparing the normal etching time. Since the device wafer is loosely bonded on the handle wafer by cool grease with several points, somewhere under the device wafer is not closely attached with the handle wafer. After the expected etching areas are etched through, the etching gas could be stored in the bonding air gap. This could be solved by characterizing the etching time and/or using SOI substrates.

In addition, to quantify the dispersion, the simulated group delays for both paths are shown in Fig. 26 with the average group delay of about 140 ps. The non-ideal fabrication effect causes large group delay variations of the mode of S_{31}.

IV. Conclusion

This paper for the first time presents the design, analysis and demonstration of a DWG based ortho-mode sub-THz interconnect channel for planar chip-to-chip communications. The detailed analyses of the single-mode transition design and the OMT design, the planar integration methods, including the dimension selection of the bending structure and backside trench, are conducted. This approach opens a new direction for high energy-efficiency high bandwidth-density chip-to-chip communications by providing multiple logical links through the same physical channel. The bandwidth density could be further boosted. Moreover, this technique can be readily scaled up to THz frequencies by scaling down the channel dimension. This results in a better energy efficiency and bandwidth density at higher frequencies.

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