Micromachined Sub-THz Interconnect Channels for Planar Silicon Processes

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Abstract — This paper presents design, fabrication and measurement results of sub-THz silicon dielectric waveguide channels for interconnect applications. To the authors' knowledge, this is the first demonstration of a sub-THz interconnect channel for planar silicon processes. The measured insertion loss peaks at -15.9 dB. Measurement results verify that the insertion loss improves by more than 35 dB compared to the scenario without channels.

***Index Terms* — Channel, dielectric waveguide, interconnect, micromachined, silicon, sub-THz, THz.**

I. Introduction

Continuous scaling of semiconductor devices allows more cores and integrated functionalities into a single chip, and supports higher processing speeds for growing computing demands of scientific and commercial workloads. This trend mandates an ever-increasing inter- and intra- chip communication bandwidth, which has been a big challenge over decades. This challenge has motivated active interconnect research to improve the performance. There are two major research thrusts in the interconnect area: electrical interconnect and optical interconnect. However, it is very challenging for both electrical interconnect and optical interconnect to address the interconnect challenges by their own. THz/sub-THz unique spectrum position, sitting between microwave and optical frequencies, allows THz/sub-THz interconnect to leverage the advantages of both electronic and optical approaches to complement them to address the interconnect issues.

To enable THz/sub-THz interconnect, low loss and silicon process compatible THz channels are one key enabling component. It not only alleviates the link budget requirement, but also leads to higher energy efficiency, one of the two most important merits for interconnect performance. With the frequency increasing, the interconnect channel size and the data throughput per channel will keep increasing. That is, the bandwidth density, the other important merit for interconnect, increases.

Low loss THz channels have been studied extensively based on a variety of materials, such as silicon ribbons [1], plastic ribbons and fibers [2], and metal wires [3]. These research results provide great evidences that THz interconnect channels can be designed with extremely low loss to enable this high potential application. However, the channels compatible with planar silicon processes are lacking of investigation in the literatures, which is one key component for THz/sub-THz interconnect.

As the first investigation effort in the planar silicon process oriented THz/sub-THz interconnect channels, this paper presents the design and fabrication of both the channel and the coupler at around 160 GHz. The reason to choose 160 GHz as the initial step is the consideration of fabrication and testing convenience. The design and fabrication methods will be further evolved to THz frequencies to support better energy efficiency and higher bandwidth density in the future.

II. Design of sub-THz Channel and Coupler

Interconnect channels and couplers compatible for planar silicon processes are crucial components for THz/sub-THz interconnect. One unique feature of such devices is that the channels need to be bended at both ends to guide the signal waves from/to the planar silicon chips. The smaller the bending radius, the larger the insertion loss it introduces. This is because a large portion of the guided signal leaks out of the channel due to a small incident angle. On the other hand, there are also constraints on the radius size from the large side. A large radius increases the channel profile, which increases the former factor and the process sensitivity to environments. Analysis indicates that the radius larger than 0.4 mm for 160 GHz signal causes < 0.8 dB insertion loss, which is adopted in our design.

To be compatible with silicon processes, high resistivity (HR) silicon dielectric material is used for the channel. Without loss of generality, Fig. 1 explains the **H** field distribution along *y* axis, *Hy*, with *Hx*=0 [4].

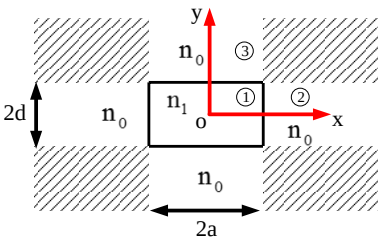

Fig. 1 Cross section view of rectangular dielectric waveguide

The **H** field distribution in different regions can represented as:

$$H_y = \begin{cases} A\cos(k_x x-\phi)\cos(k_y y-\psi) & \text{Region1} \\ A\cos(k_x a-\phi)e^{-\alpha_x (x-a)}\cos(k_y y-\psi) & \text{Region2} \\ A\cos(k_x x-\phi)\cos(k_y d-\psi)e^{-\alpha_y (y-d)} & \text{Region3} \end{cases} \quad (1)$$

where ϕ and ψ describe the phase difference corresponding to the center of waveguide along x-axis and y-axis respectively. k_x and k_y are propagation constants and α_x and α_y are the attenuation factors in the cladding material along the *x*-axis and *y*-axis, respectively. Together with boundary conditions, above

equations determine the relation between propagation constant *k*, attenuation factor α, and effective refractive index n_{eff} to characterize signal propagation along the channel.

The advantages of dielectric waveguides over metallic waveguides include: (1) lower cutoff frequencies to allow further shrinking of the channel cross-section with less performance degradation for higher bandwidth density; (2) lower losses at high frequencies for better efficiency; (3) easier integration with silicon processes without significantly increasing fabrication complexity. Besides, the large dielectric constant of silicon, around 11.9, facilitates to confine the field inside the channel to reduce propagation losses. Fig. 2(a) presents the designed silicon based dielectric channel with the bends on the two sides. Fig. 2(b) illustrates the H-distribution field on one cross section and wave propagation along the channel, which confirms that the majority of the field concentrates in the center of the channel. Fig. 2(c) describes the simulated effective index versus propagation signal frequency for the first five modes, which demonstrates the capability to support large bandwidth. Fig. 2(d) presents the simulated channel insertion loss for a 6-mm channel, < 1 dB over a broad frequency band.

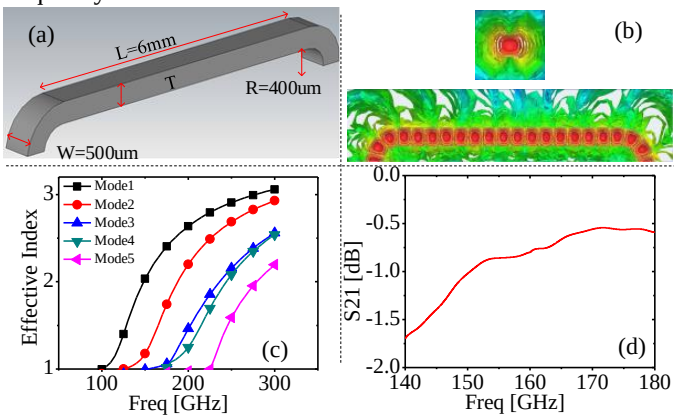

Fig. 2 (a) The designed silicon based dielectric channel for planar silicon processes; (b) the simulated H-field distribution; (c) the simulated effective index vs signal frequency for different propagation modes, and (d) the simulated insertion loss of the silicon channel

The above transmission simulation is carried out using ideal waveport in Ansys HFSS. In reality, a practical coupling structure is needed to excite the guided wave inside the Si channel. Patch antenna based structure is chosen in our work because it can generate propagation field perpendicular to the antenna plane, which is suitable to be coupled to the silicon channel. The complete structure is designed on Roger3850 substrate with 1-mil thickness, a dielectric constant of 2.9 and a loss tangent of 0.0067 at around 98 GHz. The coupling structure consists of a transition from GSG probe feeding based Coplanar Waveguide (CPW) to microstrip line, a taper for impedance matching, and a patch antenna. The dimension of the design is presented in Fig. 3(a). The complete interconnect structure, including the channel and the coupler is shown in Fig. 3(b), with channels sitting on top of the couplers vertically with a gap around 100 μm. The simulated directivity of the patch antenna is about 6.7 dBi. The total loss through the link path is approximately -5.3 dB at 160 GHz as shown in the Fig. 3(c), with the wave propagation field illustrated in Fig. 3(d).

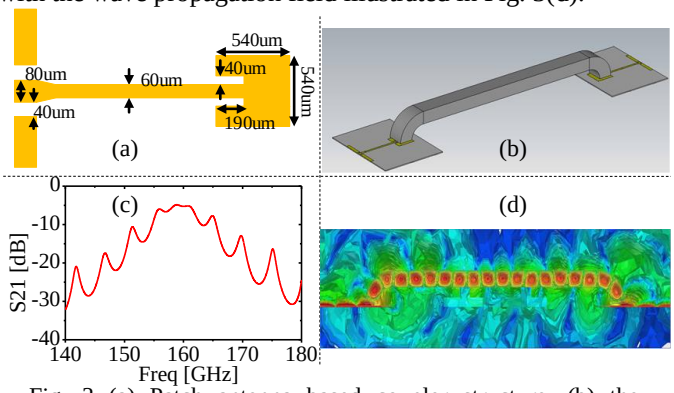

Fig. 3 (a) Patch antenna based coupler structure, (b) the complete structure of the sub-THz silicon channel with the coupler, (c) the simulated antenna gain, and (d) the simulated H-field propagation

III. Fabrication and Measurement Results

The channel is fabricated based on lithography and deep reactive ion etching (DRIE). First, a photoresist (AZ9260), which can form thick layer (around 17um), is patterned as an etching mask. Second, a HR wafer and a carrier wafer are attached together through cool grease. The silicon wave is then etched by DRIE process to generate individual channels. The antenna coupling structure is fabricated by an etch-back process on the Roger3850 substrate.

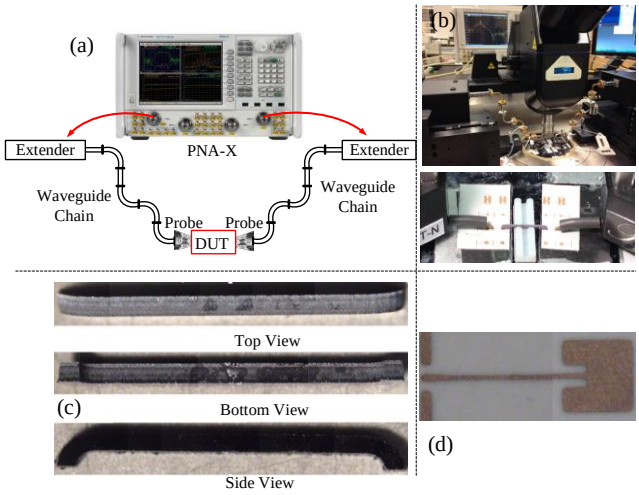

Fig. 4 (a) Measurement setup for the channel characterization, the pictures of (b) the measurement setup, (c) the fabricated channel, and (d) the fabricated patch antenna based coupler.

Fig. 4(a) illustrates the measurement structure, which is based on an Agilent PNA-X network analyzer up to 67 GHz, a pair of Virginia Diodes frequency extension modules to up-convert signal frequency to G-band: from 140 GHz to 220 GHz, and a chain of waveguides to guide the wave toward the tip of the probes. Fig. 4(b) shows the measurement setup picture with a zoom-in one at the bottom. To support the channel and facilitate alignment, a holder for the channel is created by a 3D

printer with a low dielectric constant material, about 2.7, which has negligible effects on signal propagation based on full-wave simulation. Fig. 4(c) presents the pictures of fabricated silicon waveguide channel from different perspectives. Fig 4(d) presents that the fabricated antenna coupling structure.

Fig. 5 summarizes the measurement results. Fig. 5(a) presents the return loss S_{11} of the structure, which indicates that the resonant frequency shifts to lower side and demonstrates higher return loss, which can be attributed to the coupler size offset. Fig. 5(b) presents the measured insertion loss S_{21} with and without the channel. The peak S_{21} with the channel is about -15.9 dB, while it drops to lower than -51dB when the channel is removed. Therefore, it demonstrates the improved insertion loss of more than 35 dB with the channel. To verify performance sensitivity, channels with different thickness, from 300 μm to 500 μm with a 50 μm step, have been fabricated and tested. The S_{11} is maintained very closely to each other for different thickness channels, which indicates that the frequency response is not determined by the channel, consistent with the simulation results. The magnitude of insertion loss S_{21} varies with channel thickness. The larger the thickness, the lower the insertion loss tends to be. When the thickness is larger than 450 μm, the magnitude of S21 are maintained similarly.

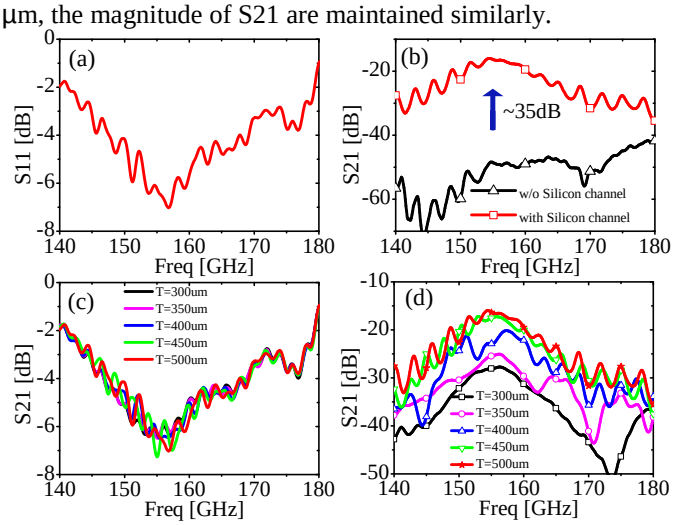

Fig. 5 (a) Measured return loss S_{11}, (b) the measured S_{21} without and with the channel, which indicates more than 35 dB improvement, and the measured (c) S_{11} and (d) S_{21} of the channels with different thickness.

In this first sub-THz interconnect channel demonstration, there are some differences between simulation and measurement results. In Fig. 6, it can be seen that the resonant frequency shifts from 160 GHz to 154 GHz. Also, the simulated S_{21} is about -5.3 dB, while the measured S_{21} is about -15.9 dB. The 10 dB extra insertion loss might result from the alignment accuracy, lower metal conductivity, larger loss tangent at higher frequencies, roughness of gold deposition, and other environment effects. Further investigation will be conducted in the future.

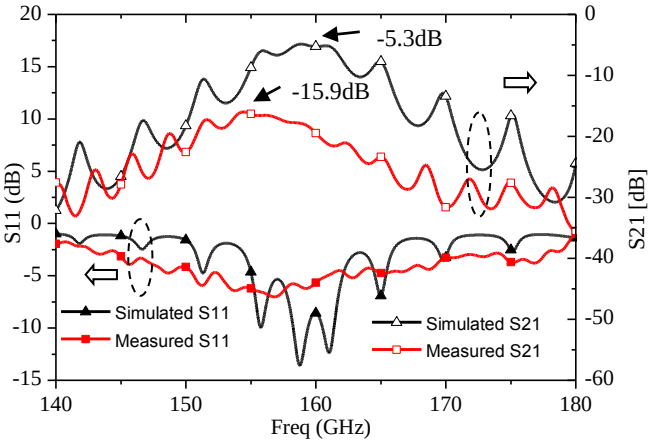

Fig. 6 Comparison between the simulated *S* Parameter and measured S Parameter. Dimensions of the channel are L=6 mm, W=500 μm, and R=400 μm.

IV. Conclusions

This paper for the first time presents a silicon based interconnect waveguide channel and coupler for planar silicon processes aiming for low cost and high reliability interconnect applications. The measurement results have validated the design concept.

Acknowledgement

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