## ABSTRACT

This tutorial will give a general walk-through of how to create a PCB and some of the issues that may arise during the process. The first and most important thing to remember is to read/watch all of Professor Liu's supplementary material including the Blinky tutorials. It allows you to become familiar with KiCad's nuances, which will allow you to save a lot of time once you begin your design.

#### THE DESIGN

#### SCHEMATIC & SCHEMATIC LIBRARY EDITOR

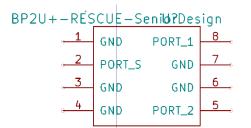
Leading up to the PCB you need to ensure that you first have a working schematic. This is done by using KiCad's schematic editor. The symbol to reach this is shown below with the symbol highlighted in blue.



Most of the components can be found in the device library such as resistors, capacitors, potentiometers etc. Utilizing the default libraries now will make association in the netlist much easier later. However, if the component isn't available then you will need to use the schematic library editor. In general, it is a good idea to include plenty of test points in your design after critical functionality for debugging if, and most likely when, the system doesn't behave as intended. To symbol to reach the library editor is shown below, highlighted in blue.



In order to create your own component use the preference tab in the schematic library editor to select the datapath to the library. The folder for the new library will need to be in the same directory as the .pro file. Select the icon to create a new component. Remember to label the component as the part number to make the design easier to read. Also, the pins must be labeled as this will be matched to the datasheet in the footprint section. Once the component is saved in the library it can be accessed in the schematic editor. Below, is an example of a custom layout for our power splitter.



When arranging the schematic, it is good practice to keep components and its biasing circuits in a modular form so when proofreading it will be less time consuming when all functions are clear and separated. An important step here is to make sure that all components include a biasing circuit (if provided in the datasheet) as well as ensuring that the bias is for the correct frequency, otherwise, the design will not perform as expected.

Once the main design is completed run an annotation, which will label components from left to right. The annotation is accessed from the schematic window shown below.

🤣 [ SeniorDesign /] (C:\Use	ers\Admin\Downloads)	
File Edit View Place Prefer	ences Tools Help	
🔺 🔒 😫 🛐 👗 🔓 🍵 🔅 [	🖲 👰 🔍 🗨 🕐 🧛 🔚 🎾 🔯 🎇 🎆	🗶 🛅 🚟 🔤 🕑 🕰
다. (슈 41 (슈)	+	Annotate schematic components

This will create a pop-up window as shown below. Click annotate and the components will automatically be labeled.

Annotate Schematic	x								
Scope									
• Use the entire schematic									
$\bigcirc$ Use the current page only									
• Keep existing annotation									
O Reset existing annotation									
$\bigcirc$ Reset, but do not swap any annotated multi-unit	parts								
Annotation Order									
<ul> <li>Sort components by X position</li> </ul>	$\mathcal{M}$								
○ Sort components by Y position	\$								
Annotation Choice									
Use first free number in schematic									
O Start to sheet number*100 and use first free num									
○ Start to sheet number*1000 and use first free nu	nber								
Dialog									
Keep this dialog open									
Always ask for confirmation									
Close Clear Annotation Annotate	h								

Next, run an electrical test. This will make sure all wires are connected and no rules are violated. Keep in mind this doesn't mean that there aren't any errors in the functionality of the design. The electrical test symbol is also in the schematic window and shown below.

y	[ SeniorDesign /] (C:\Users\Admin\Downloads)
Fil	e Edit View Place Preferences Tools Help
	£.  £ 17 ‰ 5 ≜   3 < ( 10 👰 < < < < < < < < < < < < < < < < < <
In	Perform electrical rules check
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$\Rightarrow$	

An example of an electrical test output is shown below. Most errors are just warnings and can be ignored.

Electrical Rules Checker	×
ERC Options	
ERC Report: Messages:	
Total: 10	^
Warnings: 10	
Errors: 0	
Create ERC file report	~
Error list:	
ErrType(3): Pin connected to some others pins but no pin to drive it	^
@ (506.73 mm,10.16 mm): Pin 3 (Power input) of component U6 is not driven (Net 1).  ErrType(3): Pin connected to some others pins but no pin to drive it	
ErrType(2): Pin not connected (and no connect symbol found on this pin)	
@ (485.14 mm,179.07 mm): Pin 24 (Input) of component U5 is unconnected.	
ErrType(4): Conflict problem between pins. Severity: warning	
• @ (699.77 mm,306.07 mm): Pin 1 (Power input) of component #PWR09 is connected to	
@ (339.09 mm,74.93 mm): pin 1 (Unspecified) of component U1 (net 36). <u>ErrType(4): Conflict problem between pins. Severity: warning</u>	
@ (339.09 mm,74.93 mm): Pin 1 (Unspecified) of component U1 is connected to	
• @ (419.10 mm,95.25 mm): pin 1 (Power input) of component #PWR014 (net 36).	
ErrType(4): Conflict problem between pins. Severity: warning	
<ul> <li>@ (419.10 mm,95.25 mm): Pin 1 (Power input) of component #PWR014 is connected to</li> </ul>	
• @ (538.48 mm,107.95 mm): pin GND (Unspecified) of component U8 (net 36).	
ErrType(4): Conflict problem between pins. Severity: warning • @ (538 48 mm 107 95 mm): Pin GND (Unspecified) of component U8 is connected to	~
Delete Markers     Run     Clc	20
Delete Markers Run Cic	se

As a suggestion make sure that everything on the schematic is reviewed by all team members and someone from a different group or TA. This is the easiest place to correct errors because all following steps will depend on what is present in the schematic. If you want to change anything later, you will need to edit the schematic and update the netlist and PCB.

#### NETLIST & FOOTPRINT EDITOR

After careful evaluation of the schematic and it is determined there is no error in the design go to the KiCad symbol in the schematic window and click on run CvPcb to associate component as shown below.

🖅 [ SeniorDesign /] (C:\Users\Admin\Downloads)	
File Edit View Place Preferences Tools Help	
오 🕒 🖻 🗶 🕤 🍵 🔄 💽 👰 🍳 🗨 🗛 📄 🖉 🕸	💭 🗱 🕷 🎦 🚠 🔜 📝 💭
	+ Run CvPcb to associate components and footprints
□ ☆ 4	

This will take you to the association of components called the netlist.

Housings_Dir		1.0	1 DBHZ	-			inductors_SMD:L_0603
Housings LCC		17	39nH1	-	L	:	Inductors SMD:L 0603
Housings LGA		18	39nH2	-	L	:	Inductors SMD:L 0603
Housings PGA		19	1000pF1	-	C	:	Capacitors SMD:C 0603
Housings QFP		20	1000pF2	-	C	:	Capacitors SMD:C 0603
Housings SIP		21	1000pF3	-	C	:	Capacitors SMD:C 0603
Housings SOIC		22	1000pF4	-	С	:	Capacitors SMD:C 0603
Housings SON		23	1000pF5	-	C	:	Capacitors SMD:C 0603
Housings SSOP		24	1000pF6	-	C	:	Capacitors SMD:C 0603
IR-DirectFETs		25	C1	-	C	:	Capacitors SMD:C 0603
Inductors SMD		26	C2	-	22pF	:	Capacitors_SMD:C_0603
Inductors THT		27	C3	-	4.7uF		
LEDs -		28	C4	-	.1uF	:	Capacitors SMD:C 0603
Measurement Points		29	CS	-	luF	:	Capacitors SMD:C 0603
Measurement Scales		30	C6	-	1.5pF	:	Capacitors SMD:C 0603
Microwave		31	C7	-	lnF	:	Capacitors SMD:C 0603
Modules		32	CB	-			Capacitors SMD:C 0603
Mounting Holes		33	C9	-	1nF	:	Capacitors SMD:C 0603
Opto-Devices		34	C10	-	.luF	:	Capacitors SMD:C 0603
Oscillators		35	C11	-	1nF	:	Capacitors SMD:C 0603
PFF PSF PSS Leadforms		36	C12	-	.luF	:	Capacitors SMD:C 0603
Pin Headers		37	C13	-	C	:	Capacitors SMD:C 0603
Potentiometers		38	C14	-	1nF	:	Capacitors SMD:C 0603
Power Integrations		39	C15	-	1.5pF	:	Capacitors SMD:C 0603
RF Antennas		40	C16	-	.1uF	:	Capacitors SMD:C 0603
RF Modules		41	C17	-			Capacitors SMD:C 0603
Relays SMD		42	C18	-	C	:	Capacitors SMD:C 0603
Relays THT		43	C19	-			Capacitors SMD:C 0603
Resistors SMD		44	C20	-			Capacitors SMD:C 0603
Resistors THT		45	C21	-			Capacitors SMD:C 0603
Resistors Universal		46	C22	-	0.1uF	:	Capacitors SMD:C 0603
SMD Packages		47	J1	-	Conn 01x01 Female		: Connectors: 1pin
Shielding Cabinets		48	J2	-	Conn 01x01 Female		: Connectors: 1pin
Socket Strips		49	J3	-	Conn Coaxial	:	
Sockets		50	J4	-	Conn Coaxial	:	
Symbols		51	L1	-	7.5nH	:	Inductors SMD:L 0603
TO SOT Packages SMD		52	L2	-	8.2nH	:	Inductors SMD:L 0603
TO SOT Packages THT		53	R1	-	R	:	Resistors SMD:R 0603
TerminalBlocks Phoenix		54	R2	-	R	:	Resistors SMD:R 0603
TerminalBlocks WAGO		55	R3	-	0	:	Resistors SMD:R 0603
Transformers SMD		56	R4	-	215	:	Resistors SMD:R 0603
Transformers THT		.57	R5	-	0	:	Resistors SMD:R 0603
Transistors OldSowjetAe		58	R6	-			Resistors SMD:R 0603
Valves		59	R7	-	R	:	Resistors SMD:R 0603
Varistors		60	R8	-			Resistors SMD:R 0603
Wire Connections Bridge:		61	R9	-	0	:	Resistors SMD:R 0603
Wire Pads	~	62	R10	-			Resistors SMD:R 0603
4 8 5		63	R11				Resistors SMD:R 0603

	ZIM SOCKET STRIPS:SOCKET STRIP	STRAIGHT IXAU KITCH/ UUMM
	280 Socket Strips:Socket Strip	
	281 Socket Strips:Socket Strip	
	282 Socket Strips:Socket Strip	
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	316 Socket Strips:Socket Strip	
	317 Socket Strips:Socket Strip	
	318 Socket Strips:Socket Strip	Straight 2x07 Pitch1.27mm SMD
	319 Socket Strips:Socket Strip	Straight 2x07 Pitch2.00mm
	320 Socket Strips:Socket Strip	Straight 2x07 Pitch2.00mm SMD
	321 Socket Strips:Socket Strip	Straight 2x07 Pitch2.54mm
	322 Socket Strips:Socket Strip	Straight 2x07 Pitch2.54mm SMD
	323 Socket Strips:Socket Strip	
	324 Socket Strips:Socket Strip	
	325 Socket Strips:Socket Strip	
~	326 Socket_Strips:Socket_Strip	

For this part all passive component will be using the SMD 0603 and the active components will vary with through hole and SMD. An example of the netlist component selection is shown above. If you can, choose components that are SMD because it will allow for less interference as well as be easier to use with multi-layer designs (quarter two). For the most part, the common components will be available in the libraries provided. Otherwise, you will need to create a customized footprint, which will be discussed later in this tutorial. For the components that are included click on the save footprint associate link symbol and automatic footprint association shown in the two figures below.

Cvpcb 4.0.7 Project: 'C:\Users\Admin\Downloads\SeniorDesign.pro'								
File Prefe	erences H	elp						
🎒 🔮 🔍	🔹 🗭 🚧 i	×i 🗊 🛱 🛱						
Part for	otprint ass	ociation in schem	atic component footprint fields SMD:C 0603					
Butt	3	C3 -	10nF : Capacitors SMD:C 0603					
Buzz	4	С4 -	1uF : Capacitors_SMD:C_0603					
Capa	5	С5 -	10nF : Capacitors SMD:C 0603					

Cvpc	Cvpcb 4.0.7 Project: 'C:\Users\Admin\Downloads\SeniorDesign.pro'									
File Prefe	erences	Help								
≙ © 0	**	vi 🗱 📰 🛱								
Batt 🗸	1	C1 -	10nF · Capacitors_SMD:C_0603							
Butt	2	Perform automatic	footprint association pacitors_SMD:C_0603							
Butt	3	СЗ -	10nF : Capacitors SMD:C 0603							
Buzz	4	C4 -	1uF : Capacitors_SMD:C_0603							
Capa	5	С5 -	10nF : Capacitors SMD:C 0603							
Capa	6	сб -	C : Capacitors_SMD:C_0603							
Capa	7	C7 -	10nF : Capacitors_SMD:C_0603							
Conn	8	C8 -	10nF : Capacitors_SMD:C_0603							
Conr	9	С9 -	C : Capacitors SMD:C 0603							

To make sure that the footprints have been saved go back to the schematic editor and click on the generate netlist symbol shown below.

Edit	View	Place	Pretere	nces	Tools	s He	elp				
8   8	r   📈		🔶 👌 🚺	۹ 📎		• P		🔎   💓 💓 🞇	₽ <sup>0?A</sup> 🕷		EOM BACK
										(	Generate netlist

If the association has worked then clicking on the component properties in the schematic will now show the associated footprint. An example of what this should look like is below.

<b>Component Properties</b>				-	•	×
Component	Fields					
Unit	Name	Value	Но	riz. Justif	y Vert.	Justify
A ~	Reference		0	Left	ОВ	ottom
Orientation (Degrees)	Value	7.5nH	•	Center	• C	enter
○ 0		Inductors_SMD:L_0603	0	Right	Отс	
○ +90	Datasheet			rugin		Υ <b>Ρ</b>
<ul><li>180</li></ul>						
○ -90			Vis	ibility	Style:	
				Show	• N	ormal
Mirror				Rotate	⊖ Ita	alic
<ul> <li>Normal</li> </ul>					OB	
O Mirror						old Itali
O Mirror					ОВ	old Itali
			Field	d Name		
Converted Shape Chip Name			Foo	otprint		
				d Value		
L			Ind	uctors_S	MD:L_060	03
Test Select				Assigr	n Footpri	nt
Timestamp			Size	1.270		mm
5A72544F			Pos	× 0.000		mm
Reset to Library Defaults		Add Field	Pos	Y 0.000		mm
		Delete Field				
		Move Up				
			C	к	Car	ncel

If your component is unique and requires a custom footprint you will need to perform similar steps as the schematic component editor. To open the footprint editor click on the symbol from the main windown as shown below.



Make sure to meticulously go over the datasheet to make sure the measurements are correct. Check to see if values are reported in mils or mms. If there are multiple pads then KiCad has a create pad array option. This allows you to set an accurate spacing between pads. To access this option, you must first lay a pad down and then right click. Click on create pad array and a pop-up window like the one shown below should appear.

Create Array	,	1.1				
Grid Array	Circular	Array				
Horizonta	l count:	5	]	Pad Numbering Direction	n	
Vertica	l count:	5	]	<ul> <li>Horizontal, then verti</li> </ul>	cal	
Horizontal s	pacing:	5	mm	<ul> <li>Vertical, then horizon</li> </ul>	tal	
Vertical s	pacing:	5	mm			
Horizonta	l offset:	0	mm	Reverse pad numberin Initial pad number	ig on alternate ro	ows or column
Vertica	l offset:	0	mm			
s	Stagger:	1		O Use first free number		
Stagger Typ	be			From start value		
				Pad Numbering Scheme		
<ul> <li>Column</li> </ul>	is			O Continuous (1, 2, 3)		
				• Coordinate (A1, A2,	. B1,)	
				Primary axis numbering:		
				Numerals (0,1,2,,9,10)		
				Secondary axis numberin	g:	
				Numerals (0,1,2,,9,10)		
				Pad numbering start: 1	1	
					ОК	Cancel

Make sure to check the datasheet to see if the component package is SMD or through hold and make that selection. Again save this component in the same directory (it should be .pretty format). You will now be able to place the component in the PCB editor.

### PCB

The PCB window is accessed by clicking on the PCB symbol as shown below, highlighted in blue.



This will pop up a blank window in which you will need to click on the generate netlist again. This will connect the footprints with the schematic components. All of the components will originally be placed on top of each other, so you will need to right click to spread them out. You will notice the pin

connections from the schematic are shown in the PCB as wires connecting. This is why it is critical to complete all edits and update the schematic or else it won't be updated in the final PCB product.

Since we are using RF components we will need to have impedance matching in our traces. This can be completed by using KiCad's PCB calculator, which can be found on the original screen as shown below.



The PCB should begin with edge cuts. In quarter 1 these dimensions are given so start with these outlines. For quarter 2, since the size will be measured it is best to have as compact a system as possible without forfeiting functionality. These edge cuts will also be required for DFM reports.

<b>.</b>	PC	B Calculator	- • ×
Regulators Track Width Electrical Spacing T	ransLine RF Attenuators Color Code Board C	lasses	
Transmission Line Type:	Substrate Parameters	Physical Parameters	
O Microstrip Line	Er 4.5	W 54.032	mil 👻 🖲
Coplanar wave guide	TanD 0.02	S 11.811	mil 👻 🔿
Coplanar wave guide with ground plan	Rho 1.72e-008	L 12.4872	mm ¥
🔿 Rectangular Waveguide	H 57	mil ×	Synthetize 🎓
🔾 Coaxial Line	T 2	mil v Electrical Parameters:	
Coupled Microstrip Line	mu Rel C 1	Z0 50	Ohm 🗸
Stripline			
O Twisted Pair		Ang_I 1	Radian 👻
S W S I I I H	Frequency 2.4	GHz GHz GHz GHz GHz GHz GHz GHz	

For our design, we will be using a coplanar waveguide with a ground plane. As shown below, you will

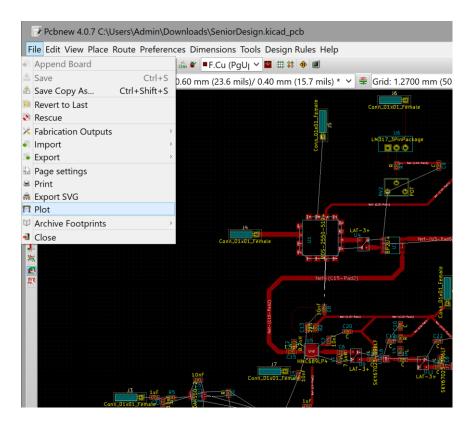
need to choose the thickness of the board which has limited values based on manufactures specs. We used 0.62 in. The dielectric spacing is given by the dielectric being used. This is also the value that must be used in the spacing when you do a ground fill. With length we can use 1 as this will not change the width calculation significantly. After these values are typed in we changed the width until we have outputted a value close to 50 ohms. This is the width of the trace you must use.

A good habit for RF components will be to keep them as close and straight as possible. This will allow the signal to avoid as much power consumption as well as limit interference. Having curved traces will create opportunity for more reflection in the system. After RF traces have been placed the other components only need a large enough trace for power to pass through.

Once all traces have been placed and all connections connected, a ground plane will be placed as well. Remember the spacing in the PCB calculator will be the spacing between the trace and plane. This will allow for less interference. If a ground plane is laid and any changes occur, make sure to replace the ground plane. Now vias should be placed to stich the top and bottom of the board together. Vias should especially be placed near RF traces and components to reduce the interference.

DFM REPORT

Once the design again has been checked multiple times by multiple people(It is good to use the checklist the professor offers) then it is ready to be checked for manufacturer issues NOT design issues. This is done by going to the plot tab in the PCB window shown below.



First the drill file will be created as shown below.

Output directory:			
			Browse
Drill Units: Millimeters Inches Zeros Format Decimal format Suppress leading zero Suppress trailing zero	Drill Map File Format: HPGL PostScript Gerber DXF SVG PDF	Info: Default Vias Drill: Use Netclasses values Micro Vias Drill: Use Netclasses values Holes Count: Plated Pads: 16 Not Plated Pads: 0	Drill File Map File Report File Close
Keep zeros  Precision  2:4	Drill File Options: Mirror y axis Minimal header Merge PTH and NPTH holes into one file	Through Vias: 0 Micro Vias: 0 Buried Vias: 0	
Messages:	Drill Origin: Absolute     Auxiliary axis		

Then the layers that should be selected are shown in the figure below ZIP the plot and drill files and then submit on the Bay AREA Circuits DFM Report. The values that are flagged here are mostly for manufacturer capabilities. Make sure the capabilities you are considering are part of the student special limits. Even if there is no error there may still be a design issue.

Gerber 🗸			Browse
Layers	Options		
<ul> <li>✓ F.Cu</li> <li>B.Cu</li> <li>B.Adhes</li> <li>F.Adhes</li> <li>B.Paste</li> <li>F.Paste</li> <li>✓ B.SilkS</li> <li>✓ F.SilkS</li> <li>✓ F.SilkS</li> <li>✓ F.Mask</li> <li>✓ F.Mask</li> <li>Dwgs.User</li> <li>Cmts.User</li> <li>Eco1.User</li> <li>Eco1.User</li> <li>Eco2.User</li> </ul>	<ul> <li>Plot sheet reference on all layers</li> <li>Plot pads on silkscreen</li> <li>Plot footprint values</li> <li>Plot footprint references</li> <li>Force plotting of invisible values/refer</li> <li>Do not tent vias</li> <li>Exclude PCB edge layer from other lay</li> <li>Mirrored plot</li> <li>Use auxiliary axis as origin</li> <li>Current solder mask settings:</li> <li>Solder mask clearance: 0 mm</li> <li>Solder mask min width: 0 mm</li> </ul>	Drill marks: None Scaling: 1:1 Plot mode: Filled Default line v 0.1	vidth (mm):
<ul> <li>✓ Edge.Cuts</li> <li>Margin</li> <li>B.CrtYd</li> <li>F.CrtYd</li> <li>B.Fab</li> <li>F.Fab</li> </ul>	Gerber Options Use Protel filename extensions Include extended attributes Subtract soldermask from silkscreen	at 5 (unit mm) 6 (unit mm)	
Messages:			
Filter: 🔽 All 🛛 🗸	Varnings 🗹 Errors 🗹 Infos 🗹 Actions	Save repo	rt to file

The DFM report will look like the figure below. Check the summary values for warnings and errors, but also check the whole report for any red boxes as these will not be within capabilities.

Name Report Generated		ort					Integ	r8tor
Peport Congrated		_	sqyuj.zip		ld.		19673 - QED OK	
Report Generated	d on		r 5, 2018 1:57:2	21 PM	Customer		InstantDFM	
Board Id								
Single PCB View -	- Original							
		Top View	v		1	Botto	m View	
1400 holds					1402 hos	2.220 PM		
PCB Size			2.2200 inc	ch x 3.4400 inch	Copper Layers			
PCB Size PCB Thickness	al - Original		2.2200 inc	h x 3.4400 inch 62.00 mil	Solder Mask			Both
PCB Size PCB Thickness Customer Panel S	al - Original		2.2200 inc	62.00 mil	Solder Mask Solder Mask Cold	Dr .		Bott
PCB Size PCB Thickness Customer Panel S SMD Pads Top	ral - Original Slze		2.2200 inc	62.00 mil 168	Solder Mask Solder Mask Cold Legend	Dr		Boti Green Top Onl
PCB Size PCB Thickness Customer Panel S SMD Pads Top SMD Pads Botton	ral - Original Size M		2.2200 inc	62.00 mil 168 0	Solder Mask Solder Mask Cold Legend Legend Color	or		Boti Greet Top Onl White
PCB Size PCB Thickness Customer Panel S SMD Pads Top SMD Pads Botton SMD Density Top	ral - Original Size m		2.2200 inc	62.00 mil 168 0 22 SMD/inch <sup>2</sup>	Solder Mask Solder Mask Colo Legend Legend Color Peeloff Mask	Dr .		Boti Greei Top Onl White None
PCB Size PCB Thickness Customer Panel S SMD Pads Top SMD Pads Botton SMD Density Top SMD Density Bott	ral - Original Size m		2.2200 inc	62.00 mil 168 0 22 SMD/inch <sup>2</sup> 0 SMD/inch <sup>2</sup>	Solder Mask Solder Mask Colo Legend Legend Color Peeloff Mask Carbon Mask			Boti Greer Top On! White None None
PCB Size PCB Thickness Customer Panel S SMD Pads Top SMD Pads Botton SMD Density Top SMD Density Bott Number of Nets	ral - Original Size m		2.2200 inc	62.00 mil 168 0 22 SMD/inch <sup>2</sup> 0 SMD/inch <sup>2</sup> 51	Solder Mask Solder Mask Cold Legend Color Peeloff Mask Carbon Mask Drill Hole Density	, ,		Boti Gree Top Onl White None 18 Holes/Inch
PCB Size PCB Thickness Customer Panel S SMD Pads Top SMD Pads Botton SMD Density Top SMD Density Bott Number of Nets Electrical Test	al - Original Size m tom		2.2200 inc	62.00 mil 168 0 22 SMD/inch <sup>2</sup> 0 SMD/inch <sup>2</sup> 51 Single Sided	Solder Mask Solder Mask Cold Legend Legend Color Peeloff Mask Carbon Mask Drill Hole Density Holes in SMD Pa	r ds		Bott Greet Top Only White None 18 Holes/Inch
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# SUGGESTIONS

- Don't wait until last minute for Quarter 1 PCB Design. It seems like you have a lot of time, but there are a lot of small technical details to implement. Once the first PCB is due the next two will be due directly after and there will be little time to figure out issues.
- It is crucial to get a good review team. Even with multiple meticulous reviews something can always be found by another pair of eyes. Just make sure your review team will take the time to really review your PCB.
- Learning hotkeys will allow you to save a lot of time on designing and editing schematics.

- Review datasheets multiple times to make sure pads are the correct size and in the right measurement unit (mm or mil). Also, make sure the footprint pad numbers match the same pin numbers in the schematic.
- The SMA footprint provided is an aerial view of the connection and not the side view. Keep this in mind while selecting a footprint for the SMA in the netlist.
- Avoid using 90° T connections in the PCB
- Use plenty of vias.
- It may help to use a socket connector instead of to directly solder some of the more sensitive components, so they don't burn out. This also will input more interference into the system so weigh the options to decide what option is superior for your system.