# **Application Note: PCB Design Using KiCad**

# Introduction

The purpose of this application note is to go over the process in designing a printed circuit board (PCB) using the CAD tool KiCad.



# **Schematic Library Editor**

The first step in designing a PCB is to obtain a schematic drawing for each component required for your project. For commonly used components such as resistors, KiCad already has the schematic included in its library. For less common components, the drawing will have to be custom made using the schematic library editor.

An example of a custom made component is the SIM-43LH+ Mixer. Pull up the datasheet for the component and look for the pin assignments. Take note of the pin name as well as the pin number.

LO	8
RF	4
IF	2
GROUND	1,3,5,6,7

## Fig 1. SIM-43LH+ Pin Connections

For pin assignments with multiple pin numbers, a good design decision may be to use only one of the pin numbers in the drawing. This will reduce the number of wires coming out of the component in the schematic and make the schematic much neater.



## Fig 2. SIM-43LH+ Schematic Drawing

For the SIM-43LH+, the ground pins are all assigned to pin number one. The pins name as well as the pin number for the remaining assignments are kept the same as the datasheet pin connection data. This is important for consistency and will help tie the schematic to the corresponding footprint at a later step.

Pin Properties				×
Pin name:	GND	Name text size:	1.270	millimeters
Pin number:	1	Number text size:	1.270	millimeters
Orientation:	⊶ Right ~	Length:	5.080	millimeters
Electrical type:	H Passive ~	]		
Graphic Style:	⊢ Line ~	]		
	to all units in component to all body styles (DeMorgan) operties	<b>1</b>		GND
			ОК	Cancel

## Fig 3. GND Pin Properties

The orientation for each pin should be selected to minimize wire overlapping on the schematic drawing for readability. The electrical type as well as the graphic style of the pin can be modified to reflect the pin design more accurately but keeping it as the default values is fine as well.



# Eschema – Electronic Schematic Editor

Once all the schematic drawings for the project's components have been obtained, the next step is to layout the circuit schematic using Escehma.



Fig 4. SIM-43LH+ in Schematic



Fig 5. Radar System Schematic

Place all the components onto the schematic and connect the components with the correct wiring. Fill in the correct value for components such as resistors

and capacitors. A good design decision would be to include test points at important locations in the circuit. For example, a test point is placed at the output of the 5V Voltage Regulator to check for the correct voltage level during testing. Another good design decision would be to use the graphics line option to draw boundaries around the components and put labels using the text option. This greatly improves readability and can be beneficial when it comes to checking for errors in the schematic.

Annotating Schematic Components

The next step would be to annotate the components on the schematic by using the annotate schematic components option. Modify the options to your liking if you want and press annotate.

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Perform Electrical Rules Check

Finally, check the connectivity of the circuit by the perform electrical rules check option. Run the electrical rules checker and make sure there are no errors.



The next step in the design process is to associate a footprint to each component. Footprints for common components, such as the 0805 series surface mount components, may be found online. Make sure to double check the dimension of the footprints you download.

# **Outline Dimensions**

HV1195





Suggested Layout, Tolerance to be within  $\pm.002$ 

CASE#	Α	В	С	D	Е	F	G	Н	J	K	L	М	Ν
101105	0.200												0.065
HV1195	(5.08)	(4.57)	(2.21)	(0.64)	(1.27)	(0.71)	(1.09)	(1.27)	(0.76)	(1.52)	(6.05)	(3.66)	(1.65)

CASE# WT, GRAM HV1195 .08

Dimensions are in inches (mm). Tolerances: 2 Pl. ± .01; 3 Pl. ± .005

Fig 6. SIM-43LH+ PCB Land Pattern

When designing your own footprints, first pull up the datasheet for the component. Most datasheets will include the PCB land pattern but if it does not, do a search for the case style of the component. The PCB land pattern should include information on various dimensions of the shape. Take special note of the unit of the dimensions. For certain PCB land patterns, the dimensions may be listed as a range to account for manufacturing tolerance. It is best to use the average value in those cases.



Fig 7. SIM-43LH+ Footprint

A good idea is to first draw a border for the footprint to help determine the placement for the pads. For the design above, the border was drawn in the CrtYd layer. You may opt to use the SilkS layer instead if you want a visible border on the PCB. For complex shapes, you would need to break down the land pattern into basic shapes since you are limited to circles, ovals, rectangles, and trapezoids. Plan how you would break down the land pattern into the available shapes if required.

Pad Properties

General Local	Clearar	nce and Settings						
Pad number:	þ			Drill				
Net name:				Shape:	Circular hole 🛛 🗸			
Pad type:	SMD		$\sim$	Size X:		mm		
Shape:	Recta	ngular	$\sim$	Size Y:	0	mm		
Position X:		0	mm	Layers				
Position Y:		0	mm	Сорре	r: F.Cu	$\sim$		
Size X:		4.57	mm	Tech	nical Layers			
Size Y:		1.27	mm		Adhes Adhes			
Orientation:		0 ~	deg		Adnes Paste			
		0	0.1 deg		Paste			
Shape offset X	¢:	0	mm		SilkS SilkS			
Shape offset Y	<i>(</i> :	0	mm		Mask			
Pad to die len	gth:	0	mm		Mask wgs.User			
Trapezoid delt	ta:	0	mm		:o1.User			
Trapezoid dire	ection:	Vert. ~		Ec	:o2.User			
Parent footpr		entation						
Rotation: 0 Board side: F		de						
board side: F	Tont SI	ue						
							OK	Cancel

#### Fig 8. A Sim-43LH+ Pad Properties

For each pad, select the appropriate pad type as well as the shape. Input the dimensions from the datasheet taking special note of unit of the dimensions. Match the pad number with the corresponding pad number on the schematic drawing. Do this for each pad and place each pad into the correct position. Use the border of the footprint as a reference when determining the position of the pads.



Once all the footprints have been designed, go back to Eschema and associate the footprints using CvPcb.

61	U2 -	-	Teensy3.2	:	Q2Footprint:Teensy3.2
62	U3 ·	-	SMA	:	Q2Footprint:SMA
63	U4 ·	-	ROS-2536C-119+	:	Q2Footprint:ROS-2536C-119+
64	U5 ·	-	PMA4-33GLN+	:	Q2Footprint:PMA4-33GLN+
65	U6 -	-	PGA-103+	:	Q2Footprint:PGA-103+
66	U7 -	-	TCBT-14+	:	Q2Footprint:TCBT-14+
67	U8 -	-	SIM-43LH+	:	Q2Footprint:SIM-43LH+
68	U9 -	-	GAT-7+	:	Q2Footprint:GAT-7+
69	<b>U</b> 10 ·	-	SP-2U1+	:	Q2Footprint:SP-2U1+
70	Ull ·	-	SMA	:	Q2Footprint:SMA_Vertical
71	U12 ·	-	LT1009	:	Q2Footprint:LT1009
72	U13 ·	-	TL974	:	Q2Footprint:TL974
73	U14 ·	-	PMA4-33GLN+	:	Q2Footprint:PMA4-33GLN+

Fig 9. Associated Sim-43LH+ Footprint

First, Select the part. Next, navigate to the library where the footprints are stored and double click on the corresponding footprint. Once all the components are associated, exit out of CvPcb.

Generate Netlist

To move on to the PCB layout phase, generate a netlist using the generate netlist option. Select the Pcbnew tab and click generate. Save the .net file.



**Pcbnew – Printed Circuit Board Editor** 

Read Netlist

Read the netlist by selecting the .net file that you saved earlier, and the components should appear on the screen.



Fig 10. Imported Components



Fig 11. Arranged Components

Arrange and organize the components to what it will look like on the PCB. Follow the general design guidelines when arranging the components:

- Keep RF components close to each other.
- Arrange RF components so that RF traces are straight as possible.
- Isolate RF traces, meaning don't place any traces on the opposite plane where an RF trace exists.
- Place power lines at locations that can be easily accessed by components. A good idea would be to place a single power line down the middle/side of the board and branch out to each component.
- Keep surface mount components on one side of the board. This will make soldering with a hot plate much less troublesome.

After the components positions have been set, draw the edgecut using the graphic line option and selecting Edge.Cuts as the layer. The edgecut determines the actual border of the PCB where the manufacture cuts it.

		-		1
1.	ň.		60	H
11	- 93	8		8
1.2	2	-	-	F

PCB Calculator

To determine the width of the RF traces, use the PCB Calculator.

PCB Calculator		- 🗆 X
Regulators Track Width Electrical Spacing	TransLine RF Attenuators Color Code Boar	rd Classes
Transmission Line Type:	Substrate Parameters	Physical Parameters
<ul> <li>Microstrip Line</li> <li>Coplanar wave guide</li> <li>Coplanar wave guide with ground plane</li> <li>Rectangular Waveguide</li> <li>Coaxial Line</li> <li>Coupled Microstrip Line</li> <li>Stripline</li> <li>Twisted Pair</li> </ul>	Er       4.5          TanD       0.02          Rho       1.72e-008          H       62       mil         T       0.15       mil         mu Rel C       1	- 🕀 Analyze Synthetize 🛧
S W S	Component Parameters: Frequency 2400 MHz	Results: ErEff Conductor Losses Dielectric Losses Skin Depth

#### Fig 12. RF Trace Calculation

Select the correct transmission line type. Fill in the substrate parameters, operating frequency, spacing, and characteristic impedance. Check your PCB manufacture for data on the substrate and dimensions of the PCB. Click synthesize and take note of the track width.

# **Design Rules**

Use the design rules editor to set different nets, or routing rules, for your different traces.



# Fig 13. Design Rules Editor

For this PCB design, the default net was used for the baseband traces while the Fat net was used for RF traces. Clearance rules as well as Via and uVia data can be obtained from the PCB manufacture. Assign each trace to the correct net by setting membership status at the bottom. Once the membership for each trace has been established, you can start routing.



Fig 14. PCB Design with Added Traces

Add tracks and vias

Route by clicking on one pad and dragging the trace to the second pad. Make and angle corrections if necessary and try to smooth the RF traces.



Fig 15. RF Trace Bottleneck Example

For certain components, you may run into issues with traces being too large for the pad. To solve this issue, you would need to "bottleneck" the trace by gradually reducing the RF trace which should look like a bottleneck. The more gradual the reduction, the better.

The next step would be to place through hole vias to help isolate the RF traces and form a solid connection between the two ground planes.

Pad number:	1		Drill	
Net name:	GND		Shape: Circular hole 🗸 🗸	
Pad type:	Through-hole	~	Size X: 0.381 mm	
Shape:	Circular	~	Size Y: 0.381 mm	
Position X:	37.687	mm	Layers	
Position Y:	31.766	mm	Copper: All copper layers 🗸 🗸	
Size X:	0.762	mm	Technical Layers	
Size Y:	0.762	mm	F.Adhes	
Orientation:	0	√ deg	☐ B.Adhes ☐ F.Paste	
	0	0.1 deg	B.Paste	
Shape offset X:	0	mm	F.SilkS	
Shape offset Y:	0	mm	B.SilkS	
Pad to die leng	jth: 0	mm	B.Mask	
Trapezoid delta	a: 0	mm	Dwgs.User	
Trapezoid direc	tion: Vert.	$\sim$	Eco1.User Eco2.User	
Parent footpri	nt orientation			
Rotation: 0.				
Board side: Fr	ont side			

# Fig 16. Through Hole Via

Create a new component as such and uncheck all technical layers. Set the drill hole size as well as the pad size according to your PCB manufacture capabilities. Place the component in PCBnew, right click and edit the pad. Under net name, fill in the net for the ground plane. Copy the via and place it anywhere where required. A quicker option on duplicating the via would be to utilize the create footprint array option. To access this option, right click on the footprint and scroll down its options.



Fig 17. PCB Design with Added Through Hole Vias

Add Filled Zone

After the vias have been added, the next step is to draw the fill zone border using the add filled zone option.

**Copper Zone Properties** 

Layer:	Net:			=N	let Filtering
F.Cu	<no ne<="" td=""><td>t&gt;</td><td>~</td><td></td><td>lisplay:</td></no>	t>	~		lisplay:
B.Cu	GND				Show all (pad count) V
	/+5V /+2.5V				
		13-Pad1)		H	lidden net filter:
		14-Pad1)			Net-*
		14-Pad2)			
		16-Pad1)		- LL é	isible net filter:
		16-Pad2) 18-Pad1)			*
		4-Pad1)			
		10-Pad1)			Apply Filters
	Mat (D	7 0-41)			
Settings					
Clearance (m	m):	Pad connection:	Priority level:		Outline slope:
0.1778		Solid $\sim$	0	•	Arbitrary $\sim$
Minimum wid	dth (mm):	Thermal Reliefs	Fill mode:		Outline style:
0.1524		Antipad clearance (mm):	Polygon	$\sim$	Hatched ~
Corner smoot	thing:	0.508	Segments / 360 deg:		
None	~	Spoke width (mm):	16	$\sim$	
Chamfer dista	ance (mm):	0.508			
0					
		Export Settin	gs to Other Zones		OK Cancel
		1	-		

Fig 18. Fill Zone Options

Fill in the minimum width data based on the PCB manufacture capabilities and the same clearance you used in the PCB calculator. Set the pad connection to solid and select the ground plane net. After pressing ok, draw the ground plane border around the PCB. Repeat this for the opposite ground plane layer.

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Fig 19. PCB Design with Filled in Ground Planes

With the Add Filled Zone tool selected, right click on the PCB and select Fill or Refill All Zones.

Perform design rules checklist

Next, use the perform design rules checklist to check for any errors with the PCB.



Once the design rules checklist clears with no errors, export the PCB for the manufacture by accessing the plot option under File.

Plot

Plot format:	Output directory:	
Gerber ~	DFM/	Browse
Layers	<ul> <li>Plot footprint references</li> <li>Force plotting of invisible values/references</li> <li>Do not tent vias</li> <li>Exclude PCB edge layer from other layers</li> <li>Mirrored plot</li> <li>Negative plot</li> <li>Use auxiliary axis as origin</li> <li>Current solder mask settings:</li> <li>Solder mask clearance: 0.2 mm</li> <li>Solder mask min width: 0 mm</li> </ul>	Drill marks: None ✓ Scaling: 1:1 ✓ Plot mode: Filled ✓ Default line width (mm): 0.1
B.CrtYd F.CrtYd B.Fab F.Fab		ut (unit mm) (unit mm)
Messages: Filter: 🗹 All	☑ Warnings ☑ Errors ☑ Infos ☑ Actions	Save report to file
	Plot Generate Dri	ll File Close

# Fig 20. Plot Options

Check the layers as follows and generate the design files. In addition, click generate drill file and click drill file. Zip up all the design and drill files and send it to the PCB manufacture to be made into a PCB.

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# What I Learned

RF theory is known to be not very tangible and hard to visualize. This project introduced a real world situation where RF concepts could be applied. One such situation comes from working with RF sections of the PCB. For example, RF traces are kept straight as possible to prevent RF signals from radiating unnecessarily. This is an application of the concept that RF signals radiate when they hit discontinuities. Another example is the idea of isolating RF traces as much as possible. This comes from studying transmission lines where sections of a transmission line have capacitive and inductive characteristics. Placing transmission lines in close vicinity accentuates these parasitic characteristics in a phenomenon known as coupling.

In addition, this project exposed me to the process of designing a PCB from scratch like the design process used in the electronics industry. Becoming familiar with this process helps the transition from school to working in the industry.

#### **Suggestions**

- The PCB designs from the quarter one will most likely have issues. Pay attention and figure out what went wrong with those designs. This will save you lots of time when designing the quarter two PCB.
- Schedule meetings with Professor Liu at important stages in the PCB design to check to see if you are on track. You may discover an issue with your PCB that you may have overlooked.