# EEC 134 --- WINTER 2016

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**Application Note** 

# **Baseband Design**

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#### 1) Baseband Components

1.1 Power supply/voltage regulator

We will use a voltage regulator (LM317 IC – Figure 7) to provide a relatively stable dc voltage supply.

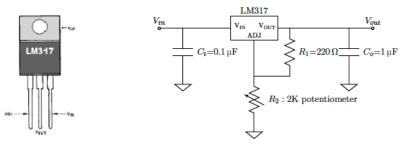


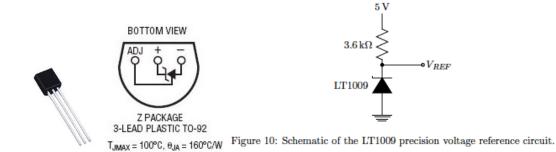
Figure 7: Pin out of the LM317 IC. Figure 8: Sc

Figure 8: Schematic of the voltage regulator circuit using LM317.

We will supply an input of 8V to get an output of 5V.

#### 1.2 Precision voltage reference

In order to present a precise and stable reference for the DAC and the ADC, we will build a precision voltage reference circuit. We will use the TI LT1009 reference IC with 2.5V output voltage.



## 1.3 Function generator

We will use a micro-controller (Teensy 3.1) and a DAC IC (MCP4921 DAC).

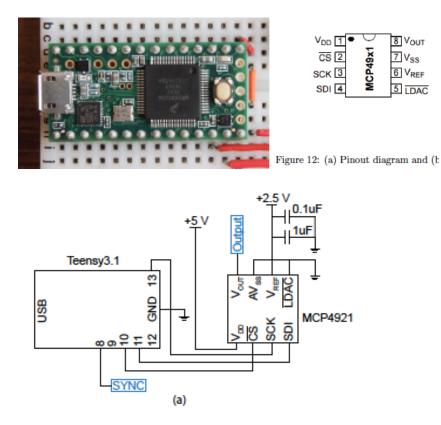


Figure 13: Schematic of the connection between the Teensy 3.1 and the MCP4921.

#### 1.4 Gain Stage + Active low-pass filter

We will implement a gain stage and an active low pass filter (LPF) with an adjustable gain using the TI TL974IN quad Op-Amp.

For the 5V supply, we will use the output of LM317 IC; and for 2.5V supply, we will use the reference voltage of LT1009.

TL974D, N, OR PW PACKAGE (TOP VIEW)									
OUT1 [ IN1- [ IN1+ [ V <sub>CC+</sub> [ IN2+ [ IN2- ]	1 2 3 4 5 6	14 13 12 11 10 9	OUT4 IN4- IN4+ V <sub>CC-</sub> IN3+ IN3-						
OUT2	7	8	OUT3						

Figure 14: Pinout diagram of the TL974 Op-Amp.

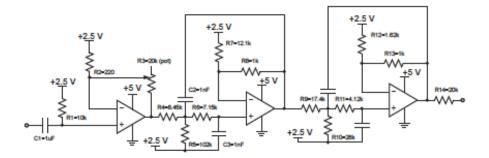


Figure 15: Schematic of the active low-pass filter.

## 2) Schematic

We will use KiCad to design the schematic and the PCB layout for the Baseband by following step by step on *The Tutorial on PCB Design* provided by Prof. Liu. In this tutorial, I will just show the tips on this Baseband PCB Design.

In the default KiCad library, we could find all the schematic symbols for the Baseband's components. However, there is not a proper schematic symbol of Teensy 3.1, so we have to create a schematic symbol for it using "Schematic library editor":

Part Library Editor no library selected File Edit View Place Preferences Hely Part Place Preferences Hely Part Place Preferences Hely Part View Place Place Preferences Hely Part View Place Preferences Hely Part View Place Place Preferences Hely Part View Place Pl	
	<ul> <li>↓</li> <li>↓</li></ul>
Z 0.26 X 266.70 Y -130.80	dx 205.70 dy -130.80 dist 297.85 mm

Figure 8: The schematic library editor program

- Click the "Create a new component" button.
- Click the "Add graphic rectangle to the component body" button and use the mouse cursor to draw a rectangle as the Figure 11 below.
- Click the "Add pins to the component" button and then add the component pins as follow the Teensy 3.1 schematic symbol below.

· · · · · · · · · · Teensy_3.1 · · · ·	• •
27 GND Vin 26	51
$\Theta = \Theta = \Theta (RX1)$ AGND $2$	-0
$\cdot \bullet \downarrow 1(TX1) \cdot \cdot$	+
2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2 2	3
• 3 3(TX) 22/A8 22	2
	La el la
• 4 4(RX) 21/A7 2	<b></b>
• • <u>5</u> 5 • • • • • • • 20/A6	<u>_</u>
6 19/A5 1	-0
• 7 7(RX3) · · · · 18/A4 18	3.
8 8(TX3) 17/A3 17	7.
	5
9 9(RX2) 16/A2	-0
• <u>10</u> 10(CS)(TX2) 15/A1	_
• • 11 11(DOUT) • • • • • 14/A0	+
12 12(DIN) 13(LED) 13	<u>3</u>
/B //B	
····· <u>\$\$568</u>	

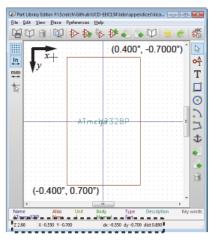


Figure 11: Drawing a rectangle in the library editor main window with the help of the built-in cordinate system.

• Then finally follow the following block diagram and the schematic for each component provided in part *1*) *Baseband Components* to draw the completed schematic for the Baseband.

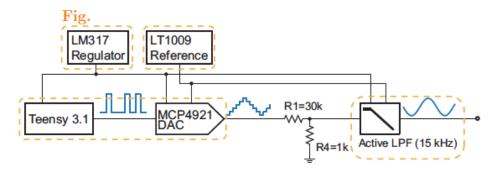


Figure 18: Block diagram of the PCB design.

• Remember to add the test points at pin #8 of the Teensy 3.1, output of MCP4921, and input of the gain stage. This will help to be easier to test the Baseband at the end.

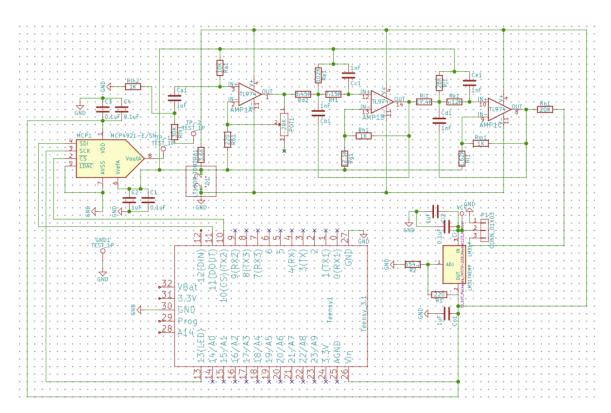
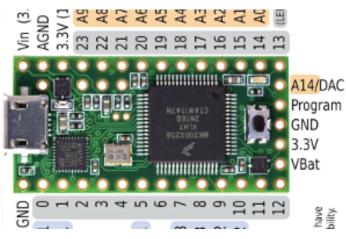


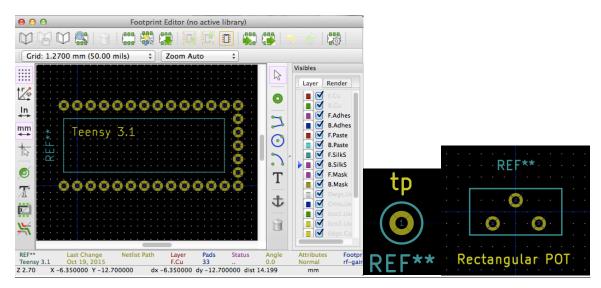
Figure A: The Final Schematic of The Baseband

# 3) PCB Design

In the KiCad library, Teensy 3.1 footprint is missing, so we have to create our own using "PCB footprint editor". Follow the steps in the PCB Tutorial and make sure that all the pads of Teensy 3.1 have the correct dimensions (drill size, pitch and row spacing).



Below is the completed footprint of the Teensy 3.1 in the Footprint Editor:



And also footprints of test point and rectangular POT.

Make sure to save it in the same directory as our project after finishing.

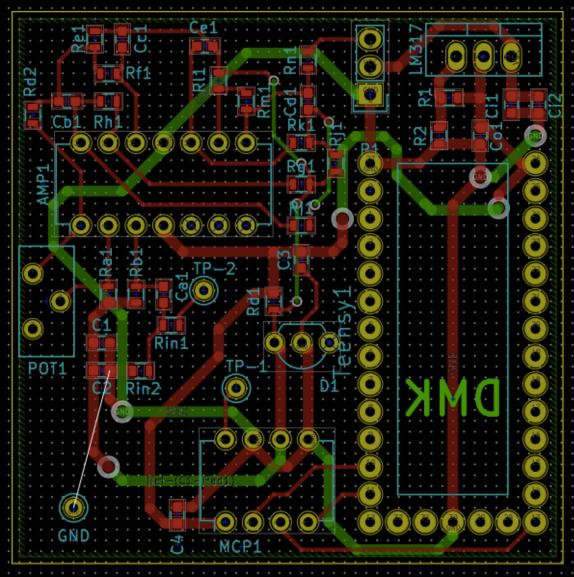
The following is the final schematic symbol and footprint association in CvPcb:

00		Cvp	cb 4.0.1-stable Pro	ject: '/Users/tntduyen92/Desktop/PCB1/PCB1.pro'	, <b>'</b>	
🖄 🕸 🔯 🔶	¥	⇒ <b>i ≱xi</b>				
Housings_SIP	Т	1 AMP1 -	- TL974	: Housings_DIP:DIP-14_W7.62mm	Г	1 rf-gain-block-footprints:adl5602
Housings_SOIC		2 C1 -	. 0.luF	: Capacitors_SMD:C_0603	11	2 rf-gain-block-footprints:cc_06031s
Housings_SSOP		3 C2 -	- luF	Capacitors_SMD:C_0603		3 rf-gain-block-footprints:LT1009
IR-DirectFETs		4 C3 -	0.luF	: Capacitors_SMD:C_0603		4 rf-gain-block-footprints:RectPOT
Inductors		5 C4 -	0.luF	: Capacitors_SMD:C_0603		5 rf-gain-block-footprints:RV2
Inductors_NEOSID		5 Cal -	luF	: Capacitors_SMD:C_0603		6 rf-gain-block-footprints:SMA
LEDs		7 Cb1 -	- 1nF	: Capacitors_SMD:C_0603		7 rf-gain-block-footprints:smd_0603
Labels		3 Cc1 -	- 1nF	: Capacitors_SMD:C_0603		8 rf-gain-block-footprints:Teensy-3.1
Measurement Points		9 Cd1 -	- lnF	Capacitors SMD:C 0603		9 rf-gain-block-footprints:tp
Measurement Scales		) Cel -	- InF	Capacitors SMD:C 0603		10 rf-gain-block-footprints:via-15mil
Mechanical Sockets		1 Ci1 -	0.luF	: Capacitors SMD:C 0603		
Microwave		2 Ci2 -	- luF	: Capacitors SMD:C 0603		
Mounting Holes		3 Col -	luF	Capacitors SMD:C 0603		
NF-Transformers ETAL		4 GND1 -	TEST 1P	rf-gain-block-footprints:tp		
Oddities		5 LM317 -		: TO SOT Packages THT: TO-220 Neutral123 Vertical		
Opto-Devices		5 MCP1 -		: Housings DIP:DIP-8 W7.62mm		
Oscillators		7 P1 -		Pin Headers: Pin Header Straight 1x03		
PFF PSF PSS Leadforms		3 POT1 -		rectPOT:RectPOT		
Pin Headers		9 R1 -		Resistors SMD:R 0603		
Potentiometers		) R2 -	654.2	Resistors SMD:R 0603		
Power Integrations		1 Ra1 -		Resistors SMD:R 0603		
Relays ThroughHole		2 Rb1 -		Resistors SMD:R 0603	0	
Resistors SMD		3 Rd1 -		Resistors SMD:R 0603		
Resistors ThroughHole		4 Rd2 -		Resistors SMD:R 0603		
Resistors Universal		5 Rel -		Resistors SMD:R 0603		
SMD Packages		5 Rf1 -		Resistors SMD:R 0603		
Socket Strips		7 Rg1 -		Resistors SMD:R 0603		
Sockets		B Rh1 -		Resistors SMD:R 0603		
Sockets BNC		9 Ril -		Resistors SMD:R 0603		
Sockets MOLEX KK-System		0 Rin1 -		Resistors SMD:R 0603		
Sockets Mini-Universal		1 Rin2 -		Resistors SMD:R 0603		
Sockets WAG0734		2 Rj1 -		Resistors SMD:R 0603		
Symbols		2 RJ1 - 3 Rk1 -		Resistors SMD:R 0603		
TO SOT Packages SMD		4 R11 -		Resistors SMD:R 0603		
TO SOT Packages THT		5 Rm1 -		Resistors SMD:R 0603		
Terminal Blocks		5 Rn1 -		Resistors SMD:R 0603		
Transformers CHK		7 Teensyl -		: Teensy:Teensy-3.1		
Transformers CHK Transformers SMPS ThroughHole		7 Teensyl - B TP-1 -		: rf-gain-block-footprints:tp		
Transformers_SMPS_Throughhole Transistors OldSowjetAera		9 TP-1 -		rr-gain-block-footprints:tp		
Valves		7 TP-2 -	TEST_IP	ri-gain-biock-rootprints(tp		
Valves	11					
Varistors Wire Connections Bridges						
Wire_Connections_Bridges Wire_Pade					1	
Components: 39, unassigned: 0	-		Filter l	iet.		Filtered by key words+library: 10
components, 55, unassigned; 0	_		ritter i	121.		Therea by Key wordsmibilary. 10

Then now is laying out the PCB:

- Click the "Generate netlist" button to generate a netlist file. Simply use the default file name and location.
- Start Pcbnew.

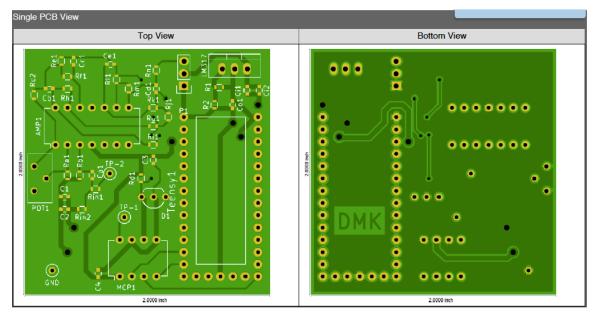
- Click the "Read Netlist" button. The "Netlist" dialog box will appear. Then Click the "Browse netlist files" button, and choose the netlist file generated from Eeschema. And then click the "Read Current Netlist" button.
- Arrangement all the components' footprints.
- Now follow the guidance of the rat's nest lines and connect the components together using copper traces. To draw a trace, Click the \Add tracks and vias" button , click on the component pin that you want the trace to start from, move the cursor to the pin that you want the trace to end, and double click to complete the trace.
- The below figure is the final PCB layout of our group baseband without a copper fill to easier to see.



• Finally, fill the PCB with copper to increase the isolation between components and provide easy access to ground. Follow step by step in the PCB tutorial.

# 4) PCB Fabrication

- After we satisfied with the PCB layout, we need to generate the artwork files for the PCB manufacturer to produce your PCB. The most common artwork file format is the Gerber format.
- To generate the Gerber files in Pcbnew, go to "Files $\rightarrow$ Plot".
- Click "Plot" to generate the Gerber files for the artwork and click "Generate Drill File" to generate the drill file (.drl) for the vias.
- Combine all these Gerber files into a .zip file.
- Then upload to Bay Area Circuits website to get the DFM Report.
- Make sure no red marks on the DFM Report then we could send all the Gerber files to Bay Area Circuit to manufacture.
- The following figure shows our group PCB Board views (Top & Bottom):



# 5) <u>Testing</u>

After the PCB boards come back, solder (SMD first and then through holes) and test the Baseband.

- a. <u>Function Generator</u>
- Open the Arduino IDE, create a new sketch, and input the code below:

#### /\*

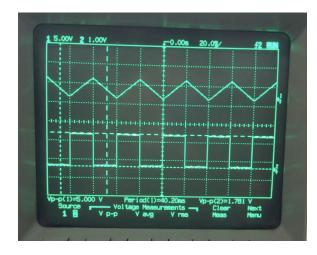
Triangle wave and sync pulse generator to control a (0-5V input range) VCO for FMCW radar.

```
The MPC4921 DAC is used to generate a triangle wave with a period of 40ms.
PWM of the Arduino UNO is use to simultaneously generate the sync pulse,
used for signal processing.
*/
#include <SPI.h> // Include the SPI library
word outputValue = 4;// A word is a 16-bit number
int incr = 1;
const int slaveSelectPin = 10; //set the slave select (chip select) pin number
const int SYNC = 8; //set the SYNC output pin number
void setup()
{
  // Set pins for output
  pinMode(SYNC, OUTPUT);
                                           // SYNC pin
  digitalWrite(SYNC, LOW);
                                      // Sync pulse low
  pinMode(slaveSelectPin, OUTPUT);
                                                  // Slave-select (SS) pin
  SPI.begin();
                              // Activate the SPI bus
  SPI.beginTransaction(SPISettings(16000000, MSBFIRST, SPI_MODE0)); // Set up the SPI
transaction; this is not very elegant as there is never a close transaction action.
}
void loop()
analogWrite(A14, outputValue);
  if (outputValue == 4040 \parallel \text{outputValue} == 0)
ł
   incr = -incr;
   digitalWrite(SYNC, !digitalRead(SYNC));
  outputValue = outputValue + incr;
  byte HighByte = highByte(outputValue); // Take the upper byte
  HighByte = 0b00001111 & HighByte; // Shift in the four upper bits (12 bit total)
  HighByte = 0b01010000 | HighByte;
                                         // Keep the Gain at 1 and the Shutdown(active low)
pin off
  byte LowByte = lowByte(outputValue); // Shift in the 8 lower bits
  digitalWrite(slaveSelectPin, LOW);
  SPI.transfer(HighByte);
                               // Send the upper byte
  SPI.transfer(LowByte);
                                // Send the lower byte
  digitalWrite(slaveSelectPin, HIGH);
                                           // Turn off the SPI transmission
}
```

 $\rightarrow$  This code will implement a triangle wave with peak to peak voltage at 5V an at period of 40ms.

- Connect the Teensy with the computer using a USB cable.
- Compile and upload the code to the Teensy.
- Record both the triangle (at VOUT) and sync (at SYNC pin#8 of Teensy 3.1) output signals on the oscilloscope. Record their amplitudes and periods.

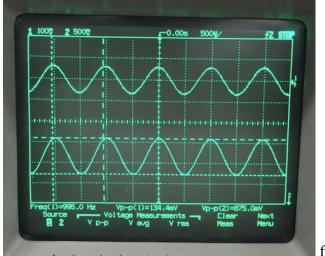
• If we get a triangle wave of 5V peak to peak and a period of 40ms and a square wave at SYNC as the following figure, our function generator worked fine.

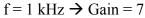


• If not, we could change the value of "int incr = 1" to get the right 40ms period and change the bits of '0' or '1' in the 2 line below to get a peak-peak voltage higher than 3V:

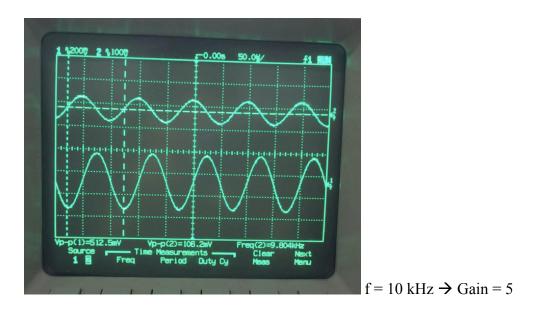
```
HighByte = 0b00001111 & HighByte; // Shift in the four upper bits (12 bit total)
HighByte = 0b01010000 | HighByte; // Keep the Gain at 1 and the Shutdown(active low)
```

- b. <u>Gain Stage + Active LPF</u>
- Use a function generator in the lab room to input to the Gain Stage + Active LPF a sine wave with Vp-p = 100mV and Frequency = 1kHz.
- Record both the input and output on the oscilloscope.

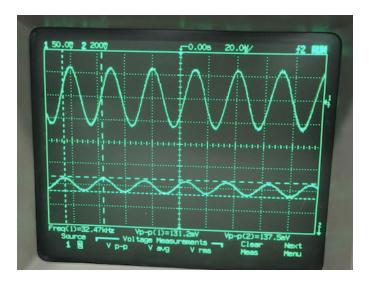




• Increase the frequency to 10 kHz:



- Finally, increase the frequency to test at what frequency the gain would be equal 1
- The following figure is recorded that our group Baseband would have a gain of 1 at frequency of 32.47 kHz.



 $\rightarrow$  If after testing, we could get the signals and gains like above figure, we could conclude that the Baseband PCB is functional.